Single Port HDMI 1.2a Receiver with Analogue Video Output

EP9851

User Guide

V0.3

Revised Date: Jun. 14, 2007

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Explore

Revision History

Version Number	Revision Date	Author	Description of Changes
0.0	Nov/08/2006	Jerry Chen	Initial Version
0.1	Apr/13/2007	Jerry Chen	Supports DAC output up to UXGA
0.2	Apr/24/2007	Ether Lai	Add register map description
0.3	Jun/23/2007	Ether Lai	Fix Typos; Add Power Sequence Notice and Power Consumption

Section 1 Introduction

1.1 Overview

EP9851 is a low cost high performance single port HDMI receiver which is compliant with HDMI 1.2a and supports Analogue Video output up to UXGA and 1080p. The chip integrates Equalizer, HDMI core and HDCP engine in a single chip.

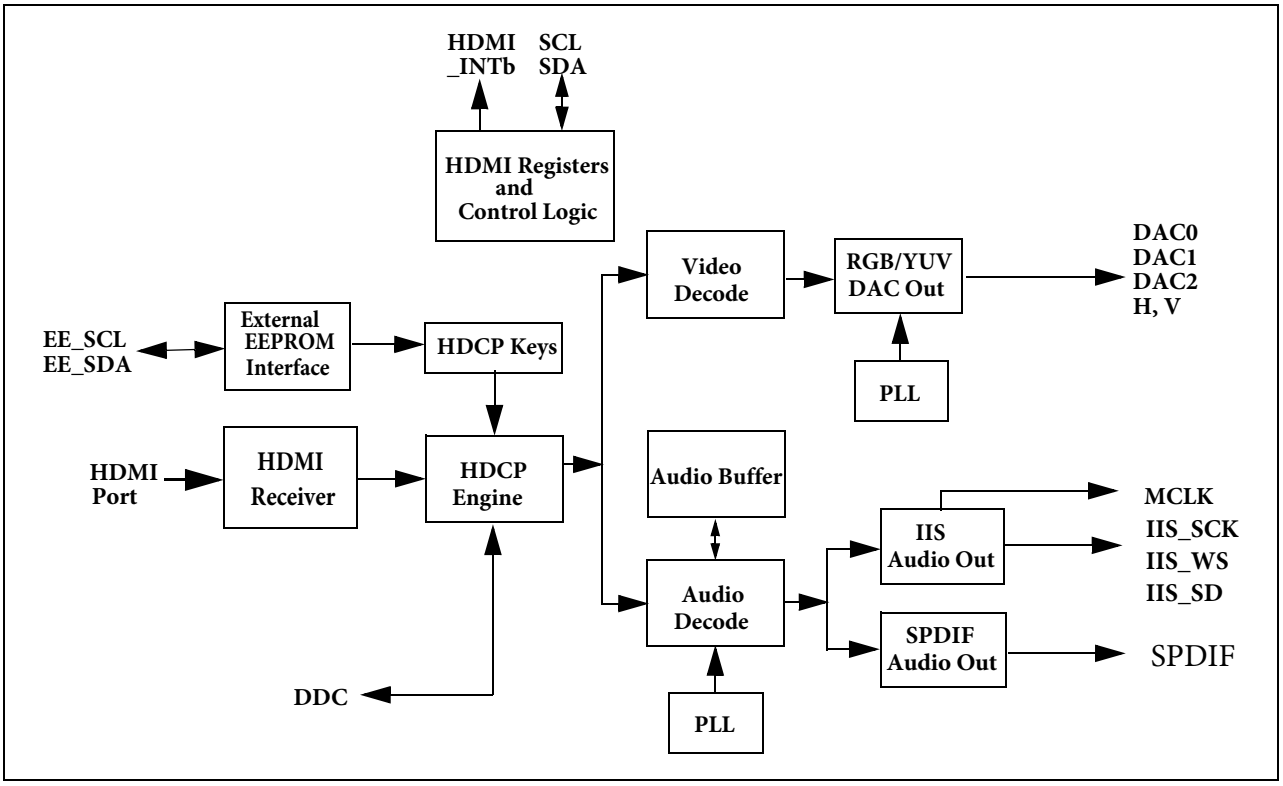
1.2 Features

- On-chip HDMI receiver with Equalizer
- On-chip HDMI Receiver core which is compliant with HDMI 1.2a specification
- On-chip HDCP Engine which supports Repeater and is compliant with HDCP 1.2 specification
- Supports pixel clock rate from 25 Mhz to 165 Mhz
- Supports Analogue Video output up to UXGA and 1080p with an on-chip 10-bit DAC
- On-chip Audio Decoder which support 2-channel IIS and S/PDIF audio outputs
- Support audio soft mute
- Support SPDIF Channel Status extraction and overwrite
- On-chip YCC422 to YCC444 conversion
- On-chip YCC to RGB and RGB to YCC conversion in ITU-R BT.601 and 709 color space
- Support Separate Sync output and Sync On Green
- Register-programmable via slave IIC interface
- Flexible interrupt registers with interrupt pin
- Link On and Valid DE Detection
- Low stand-by current (< 1mA) at power down mode
- 64-pin LQFP package

Section 2 Overview

2.1 Block Diagram

Figure 2-1 Block Diagram



2.2 Pin Diagram

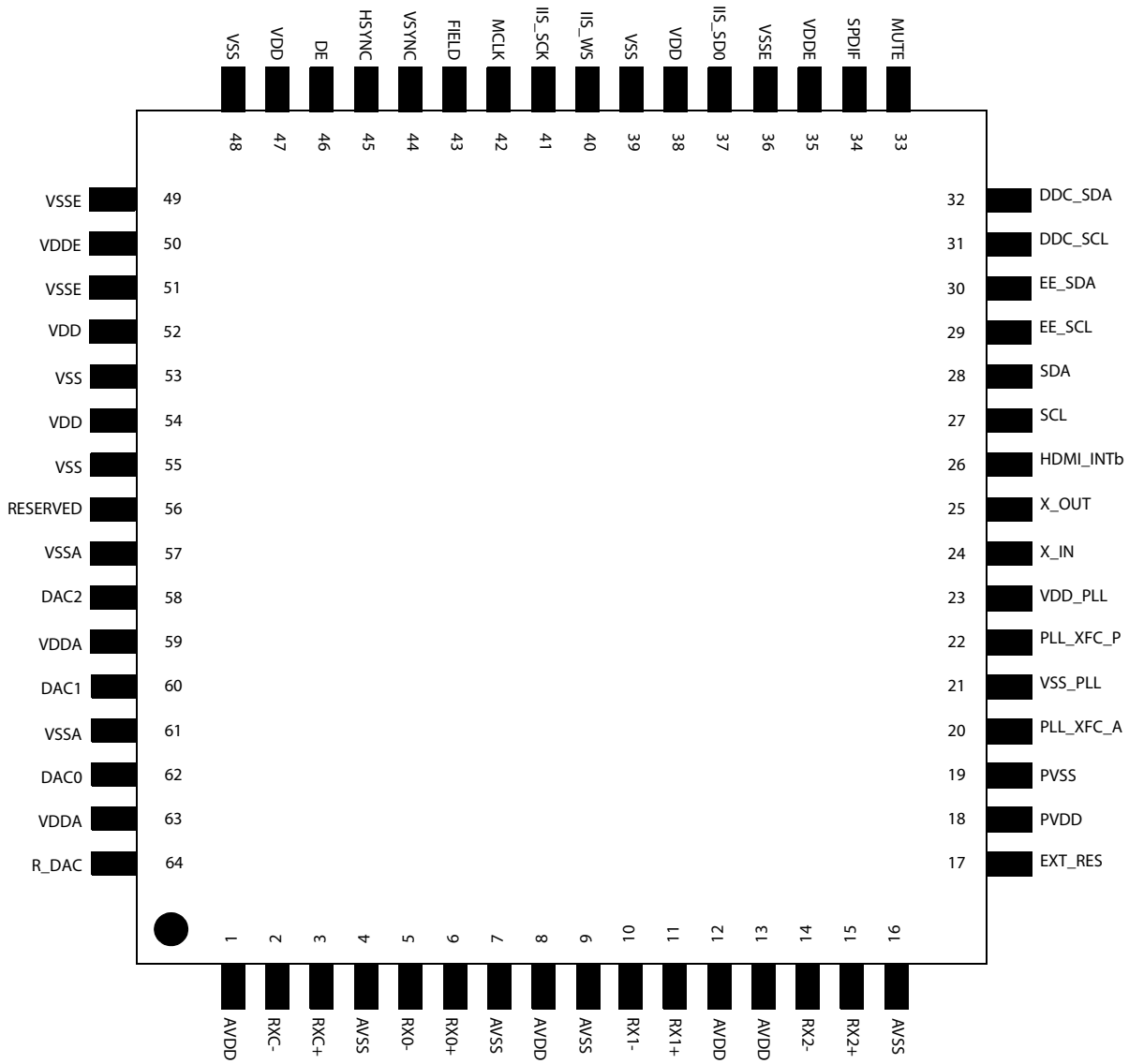


Figure 2-2 Pin Diagram

2.3 Pin Description

Unless otherwise stated, unused input pins must be tied to ground, and unused output pins left open.

Table 2-1 HDMI Receiver

Name	In/Out	Description
RXC-	IN	HDMI Receiver Differential Clock Input Pair Port 0
RXC+	IN	HDMI Receiver Differential Clock Input Pair Port 0
RX0-	IN	HDMI Receiver Differential Data Input Pair1 Port 0
RX0+	IN	HDMI Receiver Differential Data Input Pair1 Port 0
RX1-	IN	HDMI Receiver Differential Data Input Pair1 Port 0
RX1+	IN	HDMI Receiver Differential Data Input Pair1 Port 0
RX2-	IN	HDMI Receiver Differential Data Input Pair2 Port 0
RX2+	IN	HDMI Receiver Differential Data Input Pair2 Port 0
EXT_RES	IN	HDMI External Termination Resistor

Table 2-2 DDC/IIC/MCU/EEPROM

Name	In/Out	Description
HDMI_INTb	OUT	Interrupt signal (Active Low). Asserted when Information packet is received. This pin is open drain output with internal weak pull-up.
SCL	IN	SCL signal for HDMI slave IIC port
SDA	IO	SDA signal for HDMI slave IIC port
DDC_SCL	IN	IIC SCL signal for DDC Port 0
DDC_SDA	IO	IIC SDA signal for DDC Port 0
EE_SCL	OUT	SCL signal for EE IIC port
EE_SDA	IO	SDA signal for EE IIC port

Table 2-3 HDMI Output Pins

Name	In/Out	Description
MUTE	OUT	Audio Mute Output
DCLK	OUT	Data Clock Output.
VSYNC	OUT	Vertical Sync Output.
HSYNC	OUT	Horizontal Sync Output.
DE	OUT	Video Data Enable Output. When asserted, the data presents on D0, D1 and D2 pins is a valid video data.
FIELD	OUT	Field Output to indicate 1st field or 2nd field in an interlace video output. The polarity is programmable by register.
DAC0	OUT	Analogue output of B or Pb.
DAC1	OUT	Analogue output of G or Y.
DAC2	OUT	Analogue output of R or Pr.
R_DAC	Analog	For connecting a resistor to GND to set DAC output current

Table 2-4 Audio Pins

Name	In/Out	Description
MCLK	OUT	System Clock output for audio DAC (128/256/384/512 * $F_{Sampling\_Clock}$)
IIS_SCK	OUT	IIS SCK output for IIS audio ports.
IIS_WS	OUT	IIS WS output for IIS audio ports.
IIS_SD	OUT	IIS SD output for IIS audio ports.
SPDIF	OUT	SPDIF output.

Table 2-5 Misc. Pins

Name	In/Out	Description
X_IN	Analog	External Crystal Input, 18.432 Mhz
X_OUT	Analog	External Crystal Output, 18.432 Mhz
PLL_XFC_A	Analog	For connecting a capacitor to ground for on-chip PLL
PLL_XFC_P	Analog	For connecting a capacitor to ground for on-chip PLL
RESERVED	IN	Must be tied LOW for normal operation.

Table 2-6 Power Pins

Name	In/Out	Description
AVDD	PWR	HDMI Receiver Analog Power (3.3V)
AVSS	GND	HDMI Receiver Analog Ground
PVDD	PWR	HDMI Receiver PLL Analog Power
PVSS	GND	HDMI Receiver PLL Analog Ground
VDDA	PWR	DAC Power (3.3V)
VSSA	PWR	DAC Ground
VDDE	PWR	I/O VDD (3.3V)
VSSE	GND	I/O Ground
VDD	PWR	Internal Logic VDD (1.8V)
VSS	GND	Internal Logic Ground
VDD_PLL	GND	PLL VDD (3.3V)
VSS_PLL	GND	PLL Ground

2.4 Electrical Characteristics

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{cc} [1]	3.3V Supply Voltage	-0.3		4.0	V
V_{DD}1	1.8V Supply Voltage	-0.3		2.5	V
V_I	Input Voltage	-0.3		V_{cc} + 0.3	V
V_O [2]	Output Voltage	-0.3		V_{cc}+ 0.3	V
T_{STG}	Storage Temperature	-55		125	℃

NOTES:
1. Permanent device damage may occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	3.3V Supply Voltage	3.0	3.3	3.6	V
V_{DD}	1.8V Supply Voltage[1]	1.62	1.8	1.98	V
V_{CCN}	Supply Voltage Noise			100	mV_{p-p}
T_A	Ambient Temperature (with power applied)	0	25	70	℃

NOTES:
1. The 3V3 power shall come earlier than 1.8V power.

DC Digital I/O Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High-level Input Voltage		2.0			V
V_{IL}	Low-level Input Voltage				0.8	V
V_{OH}	High-level Output Voltage		2.4			V
V_{OL}	Low-level Output Voltage				0.4	V
I_{OL}	Output Leakage Current	High Impedance	-10		10	uA

DC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{ID}	Differential Input Voltage, Single Ended Amplitude			150		1000	mV
I_{PD}	Power-Down Current	PWR_UP = LOW No RXC+/- input				1	mA
I_{CCR_A}	Operating Current for DAC Analog Output (C_{LOAD} = 10pF, R_{EXT_RES} = 470 Ω)	TMDS Clock = 148.5MHz, 8-bits, Typical Pattern[1]	1.8V		40		mA
			3.3V		256		mA
		TMDS Clock = 148.5MHz, 8-bits, Worst Case Pattern[2]	1.8V		51		mA
			3.3V		256		mA
		TMDS Clock = 74.25MHz, 8-bits, Typical Pattern[1]	1.8V		21		mA
			3.3V		224		mA
		TMDS Clock = 74.25MHz, 8-bits, Worst Case Pattern[2]	1.8V		25		mA
			3.3V		224		mA

NOTES:

1. The typical Pattern contains a gray scale area, checkerboard area and text
2. Black and white checkerboard pattern, each checker is one pixel wide.

Video AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{DPS}	Intra-Pair (+ to -) Differential Input Skew				0.4	T_{bit}
T_{CCS}	Channel to Channel Differential Input Skew				1.0	T_{pixel}
T_{IJIT}	Differential Input Clock Jitter Tolerance				0.3	T_{bit}

I2S Audio AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{sck}	SCK Clock Period	C_L = 10pF		1		T_{sck}
T_{sck_d}	SCK Clock Duty Cycle	C_L = 10pF	40%		60%	T_{sck}
T_{sck_h}	SCK Clock High Time	C_L = 10pF	40%		60%	T_{sck}
T_{sck_l}	SCK Clock LOW Time	C_L = 10pF	40%		60%	T_{sck}
T_{iis_s}	SCK to SD and WS (Setup Time)	C_L = 10pF	40%		-	T_{sck}
T_{iis_h}	SCK to SD and WS (Hold Time)	C_L = 10pF	40%		-	T_{sck}

SPDIF Audio AC Specifications (under normal operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{spdif}	SPDIF Cycle Time	C_L = 10pF		1		UI
T_{spdif_d}	SPDIF Duty Cycle	C_L = 10pF	90%		110%	UI

Section 3 Functional Description

3.1 HDMI Receiver

The HDMI receiver has built-in equalizer which enables the port to receiver HDMI signals through long cable. The HDMI Receiver is compliant with HDMI 1.2a specification. It supports analogue video output up to UXGA and 1080p. It supports input pixel clock ranging from 25MHz - 165MHz.

3.2 HDCP Engine & HDCP Keys

The on-chip HDCP (High-bandwidth Digital Content Protection) engine is compliant with HDCP 1.2 specification. The HDCP keys and BKSV are downloaded from external EE at power up. The HDCP keys stored in external EE are encrypted for security purpose. The chip will decrypt the keys after download. The encryption software will be provided for free.

3.3 Video Data

Video data is decoded in RGB or YPbPr format through register control. The chip provides RGB or YPbPr analogue outputs with an on-chip 10-bit DAC. The chip provides Separate Sync outputs and programmable Sync On Green (SOG) options.

3.4 Audio Data

Audio data is extracted and decoded from HDMI data stream. The decoded audio data is buffered in an on-chip FIFO. Eight audio data channels are supported. An on-chip PLL is used to regenerate audio clock from the HDMI TMDS clock under the control of HDMI source. Digital audio signals in both IIS and SPDIF format are generated based on this regenerated audio clock.

3.5 InfoFrame Data

All types of Packet/InfoFrame data can be extracted, decoded from HDMI data stream and stored in the internal registers. The AVI (Auxiliary Video Information), Audio and MS (MPEG Source) InfoFrames are always extracted and put in dedicated buffers. Other Packet/InfoFrame type can be selectively extracted and stored in 2 shared packet buffers. Whenever an InfoFrame is received, an interrupt flag is set in an internal register and HDMI_INTb pin (active low) is asserted to signal MCU. The MCU can extract the InfoFrame content through IIC bus.

Section 4 Detail Functional Descriptions

4.1 General

The chip provides an IIC serial bus interface (SCL/SDA pins) for MCU to access the HDMI control/status registers. To access the HDMI control/status registers, the IIC address of 0x78 should be given.

Built-in control/status registers are organized by Register Sets. Each Register Set is comprised of one or more than one bytes of register. To address a register byte, a Word Address along with a Byte Address should be given. Word Address is used to address the register set and Byte Address is used to address the designated register byte within the addressed register set.

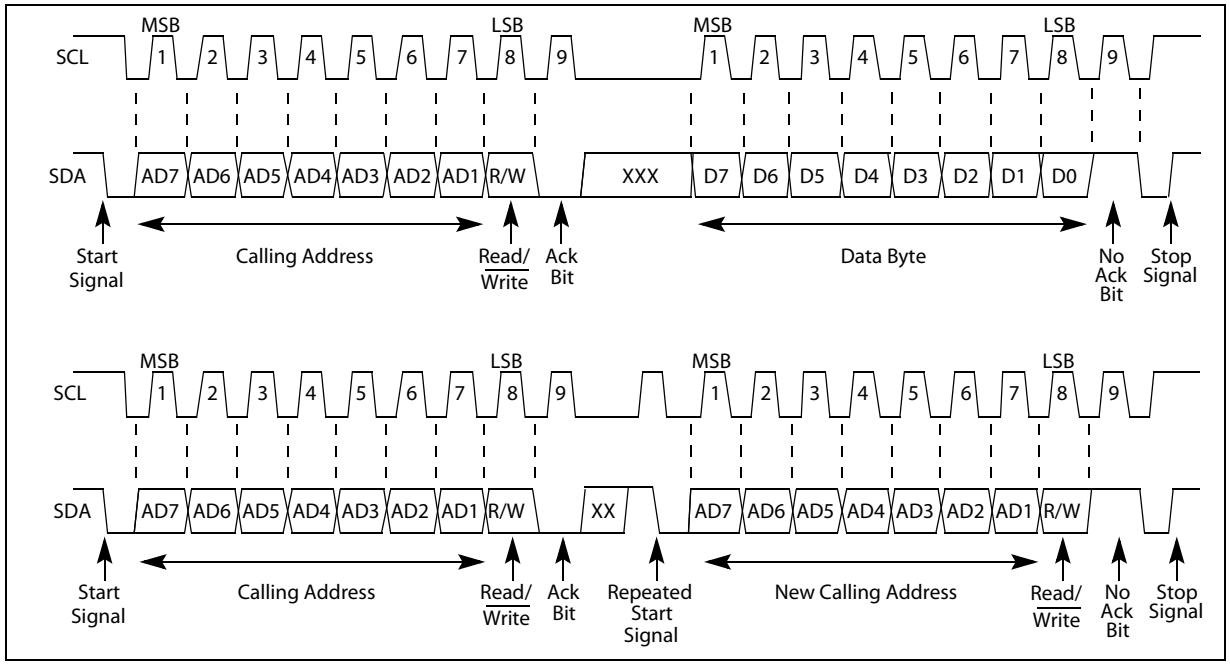
4.2 IIC Interface for HDMI control/status registers

On-chip HDMI control/status registers can be accessed by main MCU and/or the on-chip HDMI MCU through an IIC bus interface. The IIC bus is a slave (IIC address = 0x78) which uses a Serial Data line (SDA) at SDA pin and a Serial Clock Line (SCL) at SCL pin for receiving and transmitting data. All devices connected to the IIC bus must have open drain or open collector outputs. Logic AND function is exercised on both lines with external pull-up resistors, the value of these resistors is system dependent. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable at the positive edge of SCL. If the SDA changes state while SCL is HIGH, the IIC interface interprets that action as a START or STOP sequence. Data on SDA must change only when SCL is LOW.

The standard IIC traffic protocol is illustrated in the following Figure:

Figure 4-1 IIC Bus Transmission Protocol



4.2.1 Basic Protocol

There are 5 components in serial bus protocol:

- START Signal
- Slave Address Byte
- Word Address Byte for the Register Set
- Data Bytes for Read/Write from/to the Register Set
- STOP Signal

When the serial interface is inactive (SCL and SDA are HIGH), communication are initiated by a START signal which is a HIGH-to-LOW transition on SDA while SCL is HIGH. The first eight bits of data transferred after a START signal comprising a seven bit slave address (the seven MSB bits) and a single R/W bit (the LSB bit). The R/W bit indicates the direction of data transfer, "1" means read from device and "0" means write to device. If the transmitted slave address matches the address of the device, the chip sends the acknowledge by asserting SDA Low on the ninth SCL pulse. Else, the chip does not acknowledge.

On chip registers are organized by register set. Each register set is composed of single byte or multiple bytes. Each register set is assigned with a Word Address. Writing data to designated register set requires that the 8-bits Word Address of the register set is written after the slave address has been acknowledged. This Word Address selects the register set for the subsequent write operations. The write operation starts from byte 0 of the register set and continue write to the next byte of the register set if data presents. The acknowledge bit will be sent on the ninth SCL pulse after every 8-bits data received.

Data are read from address register set in a similar manner. Reading requires two IIC transfer operations:

The Word Address must be written with the R/W bit of the slave address byte being LOW to set up a sequential read operation.

Reading (the R/W bit of the slave address byte HIGH) begins at the previously established Word Address. Data is read from byte 0 of the address register set and continue the next byte read if acknowledge presents.

To terminate a read/write sequence, a STOP signal must be sent. A STOP signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a START signal without first generating a STOP signal to terminate the current read/write sequence. This can be used to change the mode of communication (read, write) between the slave and master without releasing the bus.

4.2.2 Examples of the read/write sequence

Write to a Register Set

- START Signal

- Slave Address Byte (R/W bit = LOW)
- Word Address Byte
- Data Byte/Bytes to the register set starting from byte 0
- STOP Signal

Read from a Register Set

- START Signal
- Slave Address Byte (R/W bit = LOW)
- Word Address Byte
- STOP Signal (Optional)
- START Signal
- Slave Address Byte (R/W = HIGH)
- Data Byte/Bytes from addressed register set starting from byte 0
- STOP Signal

4.3 HDMI Control/Status Registers

4.3.1 Register Descriptions

4.3.1.1 HDCP key Area (Word Address = $00 ~ $28)

Reserved.

4.3.1.2 Interrupt Flags (Word Address = $29)

Table 4-1 Interrupt Flags Register

Word Address = $29

bit	7	6	5	4	3	2	1	0
R		AVMC_F	AVMS_F	SEL2_F	SEL1_F	MS_F	ADO_F	AVI_F
	0	0	0	0	0	0	0	0

This register is Read Only. The lower 7 bits of this register (bit 6-0) are used as interrupt flags for InfoFrame and other packets. Whenever a designated packet is received, the corresponding interrupt flag bit will be set and the HDMI_INTb pin will be asserted, if the corresponding interrupt enable bit is set, to inform MCU to read this register and download the data if needed. After MCU read this register, all the flag bits will be cleared automatically. Special care is taken by the design to prevent accidentally loss of any flag bit.

AVI_F — AVI InfoFrame Interrupt Flag

This bit is set when an AVI InfoFrame is received and is auto cleared when the register is read.

ADO_F — Audio InfoFrame Interrupt Flag

This bit is set when an Audio InfoFrame is received and is auto cleared when the register is read.

MS_F — MS InfoFrame Interrupt Flag

This bit is set when an MS InfoFrame is received and is auto cleared when the register is read.

SEL1_F — 1st Selected Packet Interrupt Flag

This bit is set when the selected packet 1is received and is auto cleared when the register is read.

SEL2_F — 2nd Selected Packet Interrupt Flag

This bit is set when the selected packet 2 is received and is auto cleared when the register is read.

AVMS_F — AVMUTE Set Interrupt Flag

This bit is set when AVMUTE is set by General Control Packet and is auto cleared when the register is read.

AVMC_F — AVMUTE Clear Interrupt Flag

This bit is set when AVMUTE is cleared by General Control Packet and is auto cleared when the register is read.

4.3.1.3 Interrupt Enable Register (Word Address = $29)

Table 4-2 Interrupt Enable Register

Word Address = $29

bit	7	6	5	4	3	2	1	0
W	INT_POL	AVMC_IEN	AVMS_IEN	SEL2_IEN	SEL1_IEN	MS_IEN	ADO_IEN	AVI_IEN
Pin Reset:	0	0	0	0	0	0	0	0

This register is Write Only. The lower 7 bits of this register (bit 0-6) are used as interrupt enable bits for Interrupt flags.

INT_POL — HDMI_INTb pin polarity
1 = IHDMI_INTb pin is active high push pull.
0 = HDMI_INTb pin is active low with weak pull-up.

AVI_IEN — AVI_F interrupt enable
1 = HDMI_INTb pin will be asserted if AVI_F is set.
0 = HDMI_INTb pin is not affected by AVI_F.

ADO_IEN — ADO_F interrupt enable
1 = HDMI_INTb pin will be asserted if ADO_F is set.
0 = HDMI_INTb pin is not affected by ADO_F.

MS_IEN — MS_F interrupt enable
1 = HDMI_INTb pin will be asserted if MS_F is set.
0 = HDMI_INTb pin is not affected by MS_F.

SEL1_IEN — SEL1_F interrupt enable
1 = HDMI_INTb pin will be asserted if SEL1_F is set.
0 = HDMI_INTb pin is not affected by SEL1_F.

SEL2_IEN — SEL2_F interrupt enable
1 = HDMI_INTb pin will be asserted if SEL2_F is set.
0 = HDMI_INTb pin is not affected by SEL2_F.

AVMS_IEN — AVMS_F interrupt enable
1 = HDMI_INTb pin will be asserted if AVMS_F is set.
0 = HDMI_INTb pin is not affected by AVMS_F.

AVMC_IEN — AVMC_F interrupt enable
1 = HDMI_INTb pin will be asserted if AVMC_F is set.
0 = HDMI_INTb pin is not affected by AVMC_F.

4.3.1.4 AVI InfoFrame (Word Address = $2A)

The 15-byte AVI InfoFrame content is stored in the register set with Word Address $2A with Byte-0 being the version number, Byte-1 being the packet check sum, Byte-2 corresponding to the 1st byte of the InfoFrame and Byte-14 corresponding to the last byte of the InfoFrame.

Table 4-3 AVI InfoFrame Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x2A	0	R	Version Number							
	1		Checksum							
	2		0	Y1	Y0	A0	B1	B0	S1	S0
	3		C1	C0	M1	M0	R3	R2	R1	R0
	4		0	EC2	EC1	EC0	0	0	SC1	SC0
	5		0	VIC6	VIC5	VIC4	VIC3	VIC2	VIC1	VIC0
	6		0	0	0	0	PR3	PR2	PR1	PR0
	7		Line Number of End of Top Bar (lower 8 bits)							
	8		Line Number of End of Top Bar (upper 8 bits)							
	9		Line Number of Start of Bottom Bar (lower 8 bits)							
	10		Line Number of Start of Bottom Bar (upper 8 bits)							
	11		Pixel Number of End of Left Bar (lower 8 bits)							
	12		Pixel Number of End of Left Bar (upper 8 bits)							
	13		Pixel Number of Start of Right Bar (lower 8 bits)							
	14		Pixel Number of Start of Right Bar (upper 8 bits)							

4.3.1.5 Audio InfoFrame (Word Address = $2B)

The 7-byte Audio InfoFrame content is stored in the register set with Word Address $2B with Byte-0 being the version number, Byte-1 being the packet check sum, Byte-2 corresponding to the 1st byte of the InfoFrame and Byte-6 corresponding to the last byte of the InfoFrame.

Table 4-4 ADO InfoFrame Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x2B	0	R	Version Number							
	1		Checksum							
	2		CT3	CT2	CT1	CT0	0	CC2	CC1	CC0
	3		0	0	0	SF2	SF1	SF0	SS1	SS0
	4		0	0	0	0	0	0	0	0
	5		CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
	6		DM_INH	LSV3	LSV2	LSV1	LSV0	0	0	0

4.3.1.6 MS InfoFrame (Word Address = $2C)

The 7-byte MS InfoFrame content is stored in the register set with Word Address $2C with Byte-0 being the version number, Byte-1 being the packet check sum, Byte-2 corresponding to the 1st byte of the InfoFrame and Byte-6 corresponding to the last byte of the InfoFrame.

Table 4-5 MS InfoFrame Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x2C	0	R	Version Number							
	1		Checksum							
	2		MB#0 (MPEG Bit Rate: Hz Lower -> Upper)							
	3		MB#1							
	4		MB#2							
	5		MB#3 (Upper)							
	6		0	0	0	FR0	0	0	MF1	MF0

4.3.1.7 Selected Packet 1 (Word Address = $2D)

Any other packet with specified packet type can be extracted and stored in this register set. The specified packet type needs to be written into Byte-0. If 0 value is written, no packet will be extracted. If a packet with matched packet type is received, the 3-byte Packet Header and the 28-byte Packet Content are stored in the register set in sequence starting from Byte-0 and end at Byte-30.

4.3.1.8 Selected Packet 2 (Word Address = $2E)

Any other packet with specified packet type can be extracted and stored in this register set. The specified packet type needs to be written into Byte-0. If 0 value is written, no packet will be extracted. If a packet with matched packet type is received, the 3-byte Packet Header and the 28-byte Packet Content are stored in the register set in sequence starting from Byte-0 and end at Byte-30.

Table 4-6 Selected Packet Type 1/2 Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x2D & 0x2E	0	R/W	Packet Header 0 (HB0, Selected Packet Type)							
	1	R	Packet Header 1 (HB1)							
	2		Packet Header 2 (HB2)							
	3		Data Byte 0 (PB0 / SB0)							
	4		Data Byte 1 (PB1 / SB1)							
	5		Data Byte 2 (PB2 / SB2)							
	6		Data Byte 3 (PB3 / SB3)							
	7		Data Byte 4 (PB4 / SB4)							
	8		Data Byte 5 (PB5 / SB5)							
	9		Data Byte 6 (PB6 /SB6)							
	10		Data Byte 7 (PB7 / SB0)							
	11		Data Byte 8 (PB8 / SB1)							
	12		Data Byte 9 (PB9 / SB2)							
	13		Data Byte 10 (PB10 / SB3)							
	14		Data Byte 11 (PB11 / SB4)							
	15		Data Byte 12 (PB12 / SB5)							
	16		Data Byte 13 (PB13 / SB6)							
	17		Data Byte 14 (PB14 / SB0)							
	18		Data Byte 15 (PB15 / SB1)							
	19		Data Byte 16 (PB16 / SB2)							
	20		Data Byte 17 (PB17 / SB3)							
	21		Data Byte 18 (PB18 / SB4)							
	22		Data Byte 19 (PB19 / SB5)							
	23		Data Byte 20 (PB20 / SB6)							
	24		Data Byte 21 (PB21 / SB0)							
	25		Data Byte 22 (PB22 / SB1)							
	26		Data Byte 23 (PB23 / SB2)							
	27		Data Byte 24 (PB24 / SB3)							
	28		Data Byte 25 (PB25 / SB4)							
	29		Data Byte 26 (PB26 / SB5)							
	30		Data Byte 27 (PB27 / SB6)							

4.3.1.9 Timing registers (Word Address = $3B)

The 12-bit **APPL[11:0] (Active Pixels Per Line) register** provides number of active pixels per line information. This register is read only. The lower 8-bit is given in Byte-0. The higher 4-bit is given in Byte-1 bit 3~0.

The 10-bit **HFP[9:0] (Horizontal Front Porch) register** provides number of pixels from the end of active data to the beginning of Horizontal Sync. This register is read only. The lower 8-bit is given in Byte-2. The higher 2-bit is given in Byte-3 bit 1~0.

The 10-bit **HBP[9:0] (Horizontal Back Porch) register** provides number of pixels from the end of Horizontal Sync to the beginning of active data. This register is read only. The lower 8-bit is given in Byte-4. The higher 2-bit is given in Byte-5 bit 1~0.

The 10-bit **HPW[9:0] (Horizontal Pulse Width) register** provides Horizontal Sync pulse width in number of pixels. This register is read only. The lower 8-bit is given in Byte-6. The higher 2-bit is given in Byte-7 bit 1~0.

The 12-bit **ALPF[11:0] (Active Lines Per Frame) register** provides number of active lines per frame information. This register is read only. The lower 8-bit is given in Byte-8. The higher 4-bit is given in Byte-9 bit 3~0.

The 8-bit **VFP[7:0] (Vertical Front Porch) register** provides number of lines from the end of active data to the beginning of Vertical Sync. This register is read only and is given in Byte-10.

The 8-bit **VBP[7:0] (Vertical Back Porch) register** provides number of lines from the end of Vertical Sync to the beginning of active data. This register is read only and is given in Byte-11.

The 7-bit **VPW[6:0] (Vertical Pulse Width) register** provides Vertical Sync pulse width in number of lines. This register is read only and is given in Byte-12 bit 6~0.

The 1-bit **INTL (Interlace) register** will be 1 if the video signal is in interlace mode, and 0 otherwise. This register is read only and is given in Byte-12 bit 7.

Table 4-7 Video Timing Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x3B	0	R	Active Pixels Per Line (APPL[7:0])							
	1		0	0	0	0	APPL[11:8]			
	2		Horizontal Front Porch (HFP[7:0])							
	3		0	0	0	0	0	0	HFP[9:8]	
	4		Horizontal Back Porch (HBP[7:0])							
	5		0	0	0	0	0	0	HBP[9:8]	
	6		Horizontal Pulse Width (HPW[7:0])							
	7		0	0	0	0	0	0	HPW[9:8]	
	8		Active Lines Per Frame (ALPF[7:0])							
	9		0	0	0	0	ALPF[11:8]			
	10		Vertical Front Porch (VFP[7:0])							
	11		Vertical Back Porch (VBP[7:0])							
	12		INTL	Vertical Pulse Width (VPW[6:0])						

4.3.1.10 Status Register 0 (Word Address = $3C, Byte 0)

Table 4-8 Status Register 0

Word Address = $3C, Byte 0

	6	5	4	3	2	1	0
R	PF_R[1:0]	AVMUTE	HDMI	AUTH	ENC_EN	-	LAYOUT
W	PF_W[1:0]	AVMUTE_R					
	0 1	0	-	-	-	-	-

PF_R[1:0] — (Read Only) Pixel Frequency information derived from logic. This information is used as a reference to control the PLL band for pixel clock generation.

00 = Pixel Frequency is lower than 40 Mhz
01 = Pixel Frequency is in the range of 40 Mhz to 80 Mhz
10 = Pixel Frequency is in the range of 80 Mhz to 120 Mhz
11 = Pixel Frequency is higher than 120 Mhz

PF_W[1:0] — (Write Only) PLL band control for pixel clock generation. The PLL band should be properly selected as follows in order to generate a stable pixel clock.

00 = Pixel Frequency is lower than 40 Mhz
01 = Pixel Frequency is in the range of 40 Mhz to 80 Mhz
10 = Pixel Frequency is in the range of 80 Mhz to 120 Mhz
11 = Pixel Frequency is higher than 120 Mhz

AVMUTE — (Read Only) AVMUTE signal decoded from HDMI General Control Packet.

1 = AVMUTE is in set state.
0 = AVMUTE is in clear state.

AVMUTE _R — (Write Only) AVMUTE reset.

1 = Clear AVMUTE.
0 = No operation.

HDMI — (Read Only) HDMI/DVI signalling indicator

1 = HDMI signalling detected.
0 = DVI signalling detected.

AUTH — (Read Only) HDCP Authentication indicator

1 = Indicating HDCP Authentication is done.
0 = Indicating HDCP Authentication is not done.

ENC_EN — (Read Only) HDCP Encryption Enabled indicator

1 = Indicating incoming signal is HDCP encrypted.
0 = Indicating incoming signal is not HDCP encrypted.

LAYOUT — (Read Only) The LAYOUT bit extracted from HDMI audio packet.

1 = LAYOUT bit is 1 indicating 4 audio streams are being received.
0 = LAYOUT bit is 0 indicating 1 audio stream is being received.

4.3.1.11 Status Register 1 (Word Address = $3D, Byte 0)

Table 4-9 Status Register 1

Word Address = $3D, Byte 0

bit	7	6	5	4	3	2	1	0
R	LINK_ON	DE_VALID	-	A_UF	A_OF	-		
W								
	-	-	-	-	-	1	0	0

LINK_ON — (Read Only) Link On indicator for selected HDMI Port. Only valid when HDMI is not in power down mode.
1 = Valid clock signal detected at selected HDMI Port.
0 = No clock signal presents at selected HDMI Port.

DE_VALID — (Read Only) DE Valid indicator for HDMI receiver.
1 = Valid DE signal detected at HDMI receiver.
0 = No valid DE signal presents at HDMI receiver.

A_UF — (Read Only) Audio FIFO underflow flag. Set by audio logic. Cleared by read of Status Register 1.
1 = Audio FIFO underflow detected.
0 = Normal

A_OF — (Read Only) Audio FIFO overflow flag. Set by audio logic. Cleared by read of Status Register 1.
1 = Audio FIFO overflow detected.
0 = Normal

4.3.1.12 SPDIF Channel Status Register (Word Address = $3E)

The first 20 bits of the SPDIF Channel Status code are extracted from audio packets and put in this register set. Refer to IEC60958 specification for the detailed description of each bit.

Table 4-10 SPDIF Channel Status Registers

Word Address	Byte #		bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x3E	0	R	-	PRE[0]	-	COPY	-	PCM	-	CONSUMER
	1		-	A_MODE[1]	-	A_MODE[0]	-	PRE[2]	-	PRE[1]
	2		-	CAT_CODE[3]	-	CAT_CODE[2]	-	CAT_CODE[1]	-	CAT_CODE[0]
	3		-	CAT_CODE[7]	-	CAT_CODE[6]	-	CAT_CODE[5]	-	CAT_CODE[4]
	4		-	SRC_NUM[3]	-	SRC_NUM[2]	-	SRC_NUM[1]	-	SRC_NUM[0]

4.3.1.13 Status Register 2 (Word Address = $3F, Byte 0)

Table 4-11 Status Register 2

Word Address = $3F, Byte 0

bit	7	6	5	4	3	2	1	0
R	EE_SUM[7:0]							
W								
	-	-	-	-	-	1	0	0

EE_SUM[7:0] — (Read Only) EE Check Sum.

When EE download is completed, the 8-bit EE Check Sum is put in this register by down load logic.

4.3.1.14 General Control Register 0 (Word Address = $40, Byte 0)

Table 4-12 General Control Register 0

Word Address = $40, Byte 0

bit	7	6	5	4	3	2	1	0
R W	MUTE_POL	DDC_DIS	DE_RST_EN	HDCP_RST	SOFT_RST	PWR_DWN	reserved	
Pin Reset:	0	0	0	0	0	0	0	0

reserved— Must be programmed as 0 for normal operation

MUTE_POL — AV_MUTE output polarity control

1 = AV_MUTE pin output is active low. A low level indicate mute.

0 = AV_MUTE pin output is active high. A high level indicate mute.

DDC_DIS — Disable DDC port connection

1 = Disable DDC port connection. On-chip DDC registers are not accessible by the HDMI source.

0 = Normal.

DE_RST_EN — Enable invalid DE to reset HDCP

1 = Allow HDCP logic to be reset when invalid DE is detected. HDCP will start from non-authed and non-encrypted state after this reset.

0 = Normal.

HDCP_RST — HDCP Reset

1 = Reset the HDCP logic. HDCP will start from non-authed and non-encrypted state after this reset.

0 = Normal.

SOFT_RST — Soft Reset

1 = Reset all the HDMI and HDCP logic except IIC registers.

0 = Normal.

PWR_DWN — Power Down

1 = HDMI is in Power Down mode. HDMI and HDCP logic are reset except IIC registers
0 = Normal.

4.3.1.15 General Control Register 1 (Word Address = $41, Byte 0)

Table 4-13 General Control Register 1

Word Address = $41, Byte 0

bit	7	6	5	4	3	2	1	0
R	VPOL_R	HPOL_R	-	-	AOUT_DIS[1:0]		-	
W	VPOL_W	HPOL_W						
Pin Reset:	0	0	0	0	0	0	0	0

V_POL_R — (Read Only) HDMI VSYNC polarity detection indicator
1 = HDMI VSYNC is active low (high during active period).
0 = HDMI VSYNC is active high (low during active period).

V_POL_W — (Write Only) VSYNC output polarity control
1 = Inverse VSYNC output polarity.
0 = Normal.

H_POL_R — (Read Only) HDMI HSYNC polarity detection indicator
1 = HDMI HSYNC is active low (high during active period).
0 = HDMI HSYNC is active high (low during active period).

H_POL_W — (Write Only) HSYNC output polarity control
1 = Inverse HSYNC output polarity.
0 = Normal.

AOUT_DIS[1:0] — Audio Output Disable mode
00 = MCLK, IIS_SCK, IIS_SD, IIS_WS and SPDIF pins are normal outputs.
01 = IIS_SCK, IIS_SD, IIS_WS pins are put in tri-state with weak pull-down. MCLK and SPDIF pins are normal output.
10 = SPDIF pin is put in tri-state with weak pull-down. MCLK, IIS_SCK, IIS_SD, IIS_WS pins are normal output.
11 = MCLK, IIS_SCK, IIS_SD, IIS_WS and SPDIF pins are all put in tri-state with weak pull-down.

4.3.1.16 General Control Register 2 (Word Address = $42, Byte 0)

Table 4-14 General Control Register 2

Word Address = $42, Byte 0

bit	7	6	5	4	3	2	1	0
R W	reserved	IN422	OUT_YCC	IN_YCC	YCC_range	CS	PR[1:0]	
Pin Reset:	0	0	0	0	0	0	0	0

reserved— Must be programmed as 0 for normal operation

IN422 — Specify HDMI input format
1 = HDMI input is in 422 format
0 = HDMI input is in 444 format

OUT_YCC — Output mode control (digital output only)
1 = Digital output in YCC mode
0 = Digital output in RGB mode

IN_YCC — Specify HDMI input mode
1 = HDMI input is in YCC mode
0 = HDMI input is in RGB mode

Table 4-15 Usage of IN_YCC, IN422, OUT_YCC and OUT422

Output / Input	RGB	YCC444	YCC422
RGB	IN_YCC = 0 IN422 = 0 OUT_YCC = 0 OUT422 = 0	IN_YCC = 0 IN422 = 0 OUT_YCC = 1 OUT422 = 0	IN_YCC = 0 IN422 = 0 OUT_YCC = 1 OUT422 = 1
YCC444	IN_YCC = 1 IN422 = 0 OUT_YCC = 0 OUT422 = 0	IN_YCC = 1 IN422 = 0 OUT_YCC = 1 OUT422 = 0	IN_YCC = 1 IN422 = 0 OUT_YCC = 1 OUT422 = 1
YCC422	IN_YCC = 1 IN422 = 1 OUT_YCC = 0 OUT422 = 0	IN_YCC = 1 IN422 = 1 OUT_YCC = 1 OUT422 = 0	IN_YCC = 1 IN422 = 1 OUT_YCC = 1 OUT422 = 1

YCC_range — Data range for YCC in RGB/YCC conversion
1 = Full range YCC (0~255).
0 = Limited range YCC (16~235 for Y, 16~240 for CbCr)

CS— Color space used for RGB/YCC conversion
1 = ITU-R BT.709
0 = ITU-R BT.601

PR[1:0] — Pixel Repetition

These 2 bits control pixel repetition for Video outputs. The number of pixels to be repeated is equal to the number specified by these 2 bits plus 1. A zero value in this register means no repetition

4.3.1.17 General Control Register 3 (Word Address = $43, Byte 0)

Table 4-16 General Control Register 3

Word Address = $40, Byte 0

bit	7	6	5	4	3	2	1	0
R W	F_POL	-	-	UVSW	-	reserved	V_MUTE	A_MUTE
Pin Reset:	0	0	0	0	0	0	0	0

reserved— Must be programmed as 0 for normal operation

F_POL — Field Polarity, define the polarity of F bit in SAV/EAV code in Embedded Sync output
1 = F bit in SAV/EAV code is set in first field and cleared in second field
0 = F bit in SAV/EAV code is cleared in first field and set in second field

UVSW — UV Swap Control for YCC output
1 = UV Swap enabled
0 = Normal

V_MUTE — Video Mute Control
1 = Video is mute
0 = Normal

A_MUTE — Audio Mute Control
1 = Audio is mute
0 = Normal

4.3.1.18 General Control Register 4 (Word Address = $44, Byte 0)

Table 4-17 General Control Register 4

Word Address = $44, Byte 0

bit	7	6	5	4	3	2	1	0
R	-	-	reserved		-	SF_R[2:0]		
W						-		
Pin Reset:	0	0	0	0	0	0	1	0

reserved— Must be programmed as 0 for normal operation

SF_R[2:0] — (Read Only) Audio Sampling Frequency information derived from Audio Clock Regeneration Packet
000 = 32 KHz
001 = 44.1 KHz
010 = 48 KHz
011 = 88.2 KHz
100 = 96 KHz
101 = 176.4 KHz

110 = 192 KHz
111 = 768 KHz

4.3.1.19 General Control Register 5 (Word Address = $45, Byte 0)

Table 4-18 General Control Register 5

Word Address = $45, Byte 0

bit	7	6	5	4	3	2	1	0
R W	SCK_POL	WS_POL	WS_M	IIS_SS	reserved	AMUTE_EN	MCLK_SEL[1:0]	
Pin Reset:	0	0	0	0	0	0	0	0

SCK_POL — IIS_SCK output polarity
1 = Inverse from IIS standard.
0 = IIS standard.

WS_POL — IIS_WS output polarity
1 = Inverse from IIS standard.
0 = IIS standard.

WS_M — IIS_WS output timing mode
1 = IIS_WS is one clock delayed compared with standard IIS timing.
0 = IIS standard.

IIS_SS — IIS sample size
1 = IIS outputs 32 bits sample size.
0 = IIS outputs 16 bits sample size.

reserved — Must be programmed 0 for normal operation.

AMUTE_EN — Audio mute enable
1 = Enable audio mute when AVMUTE is set.
0 = Audio mute is not enabled.

MCLK_SEL[1:0] — MCLK Selection

These 2 bits select audio system clock (MCLK) frequency.
00 = MCLK frequency is 128 times of audio sampling frequency
01 = MCLK frequency is 256 times of audio sampling frequency. Not valid for HBR Audio.
10 = MCLK frequency is 384 times of audio sampling frequency. Not valid for HBR Audio.
11 = MCLK frequency is 512 times of audio sampling frequency. Not valid for HBR Audio.

4.3.1.20 General Control Register 6 (Word Address = $46, Byte 0)

Table 4-19 General Control Register 6

Word Address = $46, Byte 0

bit	7	6	5	4	3	2	1	0
R W	-		-		-		SD_PA[1:0]	
Reset:	1	1	1	0	0	1	0	0

SD_PA[1:0] — Audio Stream assignment for IIS_SD output

01 = Output Audio Stream 1

10 = Output Audio Stream 2

11 = Output Audio Stream 3

4.3.1.21 General Control Register 8 (Word Address = $48, Byte 0)

Table 4-20 General Control Register 8

Word Address = $48, Byte 0

bit	7	6	5	4	3	2	1	0
R W	DAC_EN	SOG_EN	reserved				reserved	reserved
Pin Reset:	0	0	0	0	0	0	0	0

reserved— Must be programmed as 0 for normal operation

DAC_EN— Video DAC output enable

1 = Enable Video DAC output.

0 = Disable Video DAC output.

SOG_EN— Sync On Green Enable

1 = Enable Sync On Green in Analogue Video output.

0 = Disable Sync On Green.

Section 5 Package