Genesys Logic, Inc.

# GL3233

## USB 3.0 Single-LUN
## Memory Card Reader Controller

## Datasheet

**Revision 1.02**
**Nov. 07, 2012**

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# Revision History

| Revision | Date | Description |
|---|---|---|
| 1.00 | 05/10/2012 | First Formal Release |
| 1.01 | 07/30/2012 | 1. Adding WHQL/WHCK Submission ID, p7<br>2. Adding LQFP 48 Pinout Diagram/Description, p7, 10, 15, 16<br>3. Adding LQFP 48 Package dimension, p25<br>4. Adding part number-GL3233-MNYXX in Chapter 8 ordering information, p26<br>5. Update SPI Flash support list in Chapter 6, p22<br>6. Adding top marking information in Chapter 7, p23, 24 |
| 1.02 | 11/07/2012 | 1. Update SPI Flash support list in Chapter 6, p22 |

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# CHAPTER 1 GENERAL DESCRIPTION

GL3233 is a crystal-less USB 3.0 Single-LUN card reader controller which can support various types of memory cards, such as CompactFlash™, Secure Digital™ (SD), SDHC, miniSD, microSD (T-Flash), MultiMediaCard™ (MMC), RS-MMC, MMCmicro, MMCmobile, Memory Stick™ (MS), Memory Stick Duo™ (MS Duo), High Speed Memory Stick™ (HS MS), Memory Stick PRO™ (MS PRO), Memory Stick PRO™ Duo (MS PRO Duo), Memory Stick PRO-HG™ (MS PRO-HG), MS PRO Micro and xD-Picture Card™ on one chip. It also supports SDXC and Memory Stick XC high density memory cards (capacity up to 2TB) and high speed SD3.0 UHS-I memory cards.

The GL3233 integrates a high speed 8051 microprocessor and a high efficiency hardware engine for the best data transfer performance between USB and various memory card interfaces. It supports ISP (In System Programming) for firmware upgrade into the external SPI Flash via USB port. It also integrates 5V to 3.3V and 3.3V to 1.2V regulators and power MOSFETs which can reduce the system BOM cost.

 

# CHAPTER 2 FEATURES

- USB specification compliance
  - Comply with Universal Serial Bus 3.0 Specification rev. 1.0 (USB 3.0)
  - Comply with Universal Serial Bus Specification rev. 2.0 (USB 2.0)
  - Comply with USB Mass Storage Class Specification rev. 1.0
  - Support USB Mass Storage Class Bulk-Only Transport (BOT)
  - Support 1 device address and up to 3 endpoints: Control (0) / Bulk Data Write Out (1) / Bulk Data Read In (2)
  - Support 5 Gbps/SuperSpeed, 480 Mbps/high-speed, and 12 Mbps/full-speed transfer rates
- Integrated USB building blocks
  - SuperSpeed/USB2.0 transceiver macro (UTM), Serial Interface Engine (SIE) and embedded Power-On Reset (POR)
- Embedded high speed 8051 micro-controller
- High efficiency hardware DMA engine improves data transfer performance between USB and flash card interfaces
- Support CompactFlash™ v6.0 with PIO mode 6 / Ultra DMA mode 7 and LBA48 (Capacity up to 144PB)
- Support Secure Digital™ v1.0 / v1.1 / v2.0/ SDHC / SDXC (capacity up to 2TB)
- Support Secure Digital™ v3.0 UHS-I (Ultra High Speed): SDR12/SDR25/SDR50/DDR50/SDR104
- Compliant with MultiMediaCard™ (MMC)
  - MMC specification v3.x / v4.0 / v4.1 / v4.2 / v4.3 / v4.4
  - x1 / x4 / x8 bit data bus
- Support Memory Stick™ / Memory Stick PRO / Memory Stick PRO Duo / Memory Stick Micro /Memory Stick PRO-HG / Memory Stick XC (capacity up to 2TB)
  - Compliant with Memory Stick Series Specification: MS v1.43, MS PRO v1.05, MS Micro v1.04 (MS HG Micro v1.00), MS PRO-HG Duo 1.03, MS XC Duo v1.00, MS XC-HG Duo v1.00, MS XC Micro v1.00 and MS XC-HG Micro v1.00
  - Support Read/Write quad data access (512Bytex4) for MS PRO-HG to enhance the transmission rate
- Support xD-Picture Card™ v1.2C Type M/H
- Support ISP (In System Programming) for firmware upgrade into the external SPI Flash via USB port
- On-Chip power MOSFETs for supplying flash media card power
- On-chip 5V to 3.3V and 3.3V to 1.2V regulator
- Support U0/U1/U2/U3 power management mode
- Support OCCS (On-Chip Clock Source) to eliminate the use of external 25MHz crystal
- Pass the USB-IF Test Procedure for SuperSpeed product (TID: 340810011)
- Pass WHCK (Windows Hardware Certification Kit) test for Windows 8 (Submission ID: 1508144)
- Pass WHQL (Windows Hardware Quality Lab) test for Windows 7 (Submission ID: 1497856)
- Available in LQFP64 pin package (7x7mm) which can support one LUN: SD/MS/xD/CF
- Available in LQFN46 pin package (6.5x4.5mm) which can support one LUN: SD/MS/xD
- Available in LQFP48 pin package (7x7mm) which can support one LUN: SD/MS/xD

 

# CHAPTER 3 PIN ASSIGNMENT

## 3.1 LQFP 64 Pinout

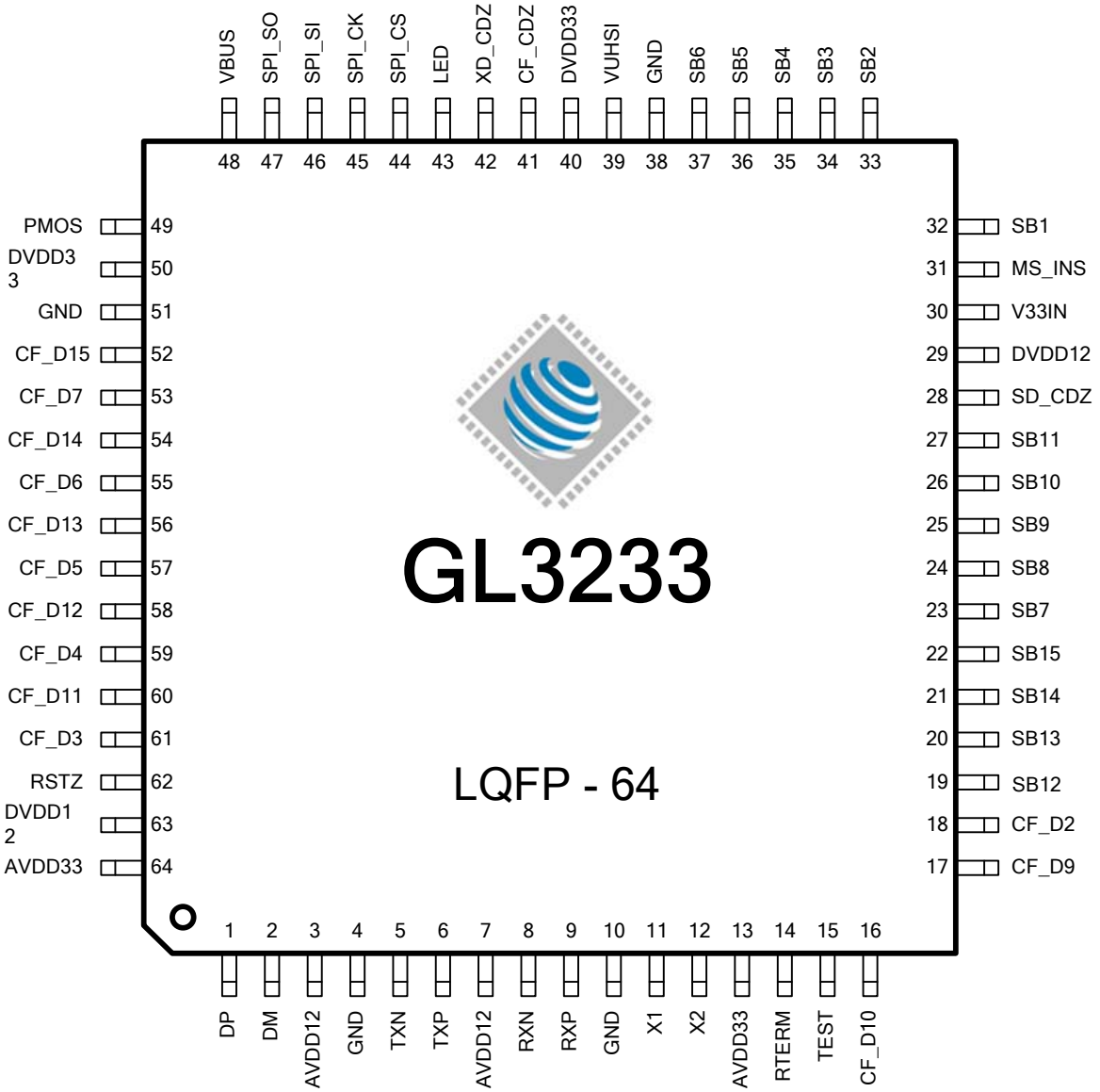


**Figure 3.1 - LQFP 64 Pinout Diagram**

 

## 3.2 LQFN 46 Pinout

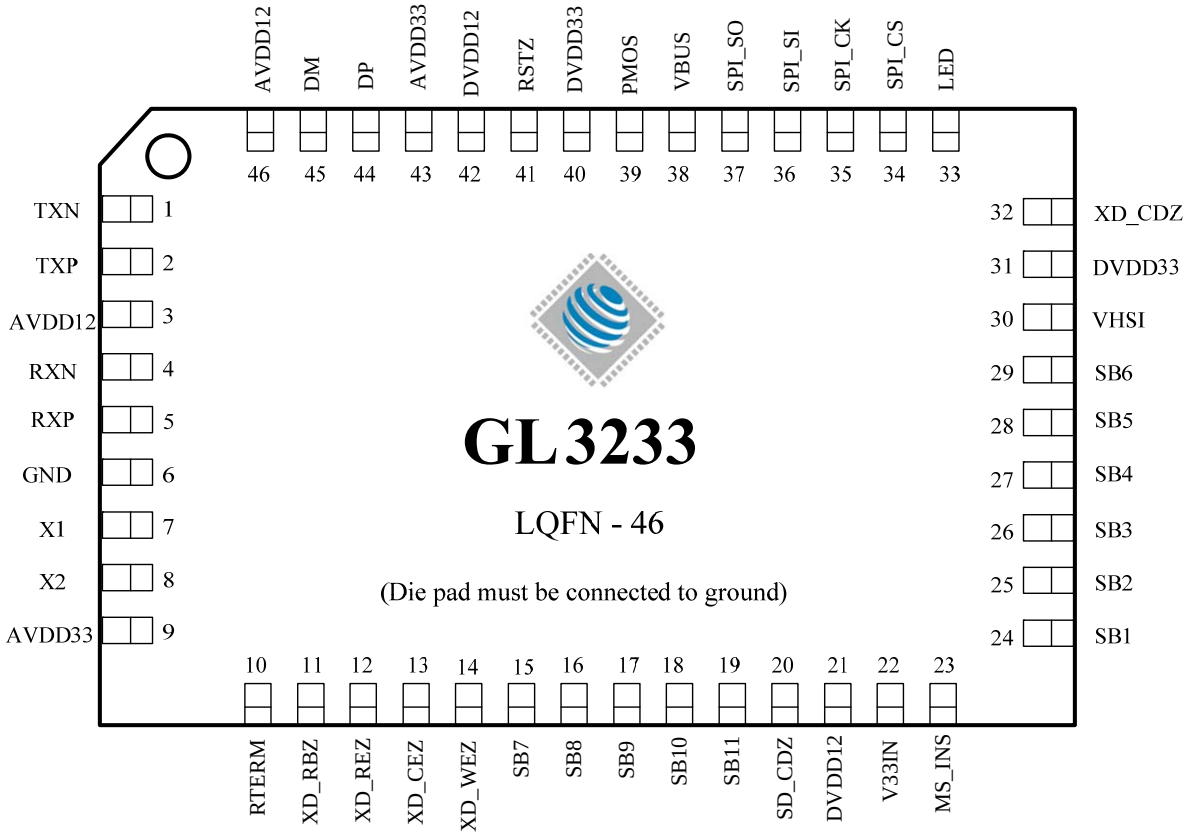


**Figure 3.2 - LQFN 46 Pinout Diagram**

## 3.3 LQFP 48 Pinout

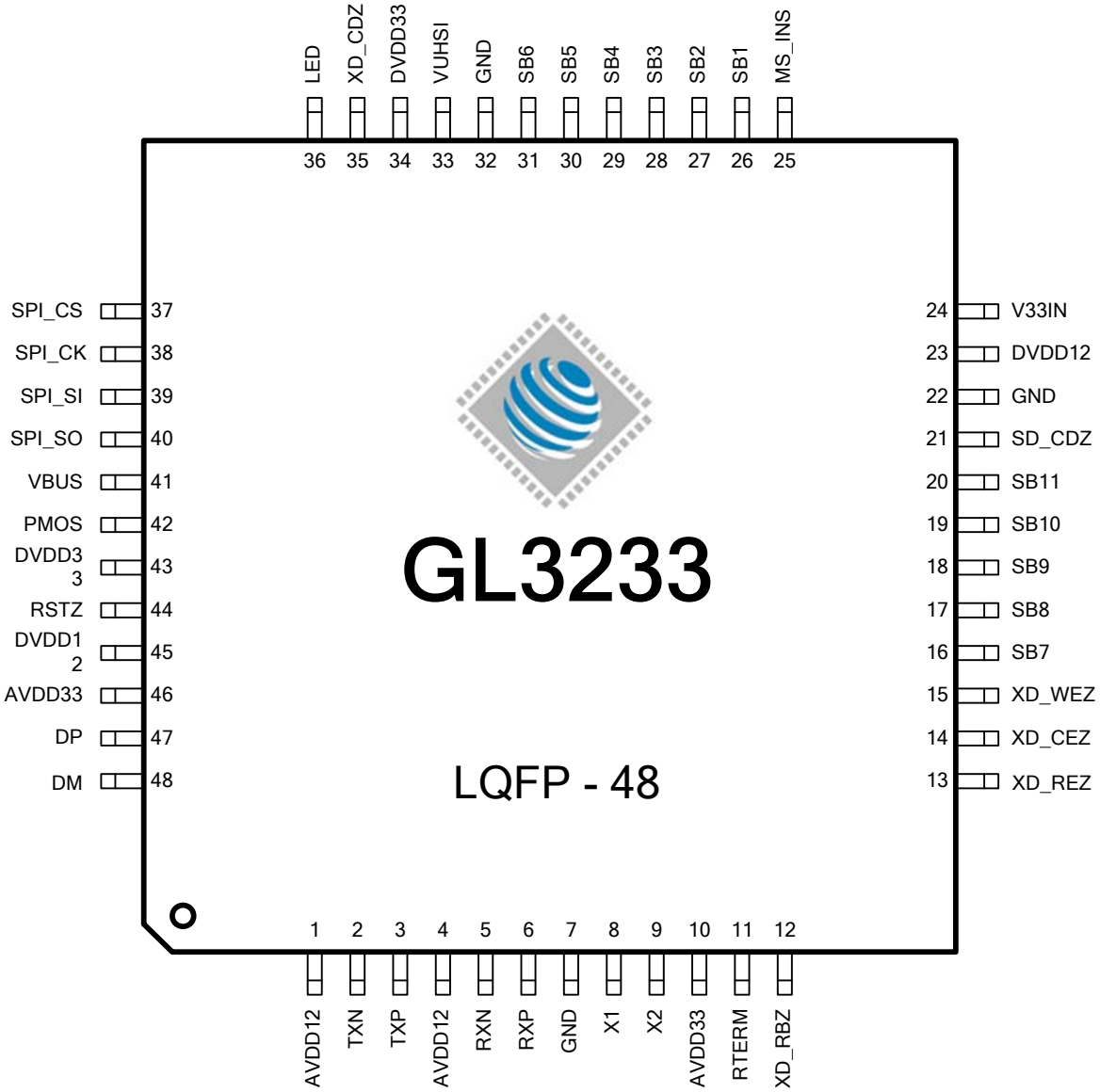


**Figure 3.3 - LQFP 48 Pinout Diagram**

## 3.4 Pin Description

**Table 3.1 – LQFP64 Pin Description**

| Pin Name | LQFP 64 Pin | Type | Description |
|---|---|---|---|
| **Power/Ground** | | | |
| AVDD12 | 3,7 | P | Analog 1.2V power source |
| AVDD33 | 13,64 | P | Analog 3.3V power source |
| DVDD12 | 29,63 | P | Digital 1.2V power source |
| DVDD33 | 40,50 | P | Digital 3.3V power source |
| V33IN | 30 | P | 3.3V to 1.2V regulator power source. Input range from 1.8V to 3.3V |
| VUHSI | 39 | P | SD 3.0 IO PAD Power, the power source of this pin comes from the internal regulator of GL3233 and no need of external power input |
| VBUS | 48 | P | 5V Power source |
| PMOS | 49 | P | Card power 900mA |
| GND | 4,10,38,51 | P | Ground |
| **USB PHY Interface** | | | |
| DP | 1 | A | USB 2.0 D+ |
| DM | 2 | A | USB 2.0 D- |
| TXN | 5 | A | USB 3.0 TX- |
| TXP | 6 | A | USB 3.0 TX+ |
| RXN | 8 | A | USB 3.0 RX- |
| RXP | 9 | A | USB 3.0 RX+ |
| RTERM | 14 | A | USB reference resistor. This pin is used to control the level of USB signal. A 680ohm, 1% resistor is recommended to be populated between RTERM and GND |
| X1 | 11 | I | 25MHz XTAL input. It can be connected to external 25MHz clock input (optional) |
| X2 | 12 | B | 25MHz XTAL output (optional) |
| **Memory Card Interface** | | | |
| SD_CDZ | 28 | I, pu | SD card detect<br>0: Card insert<br>1: No card |
| MS_INS | 31 | I, pu | MS insertion detect<br>0: Card insert<br>1: No card |
| XD_CDZ | 42 | I, pu | xD card detect<br>0: Card insert<br>1: No card |
| CF_CDZ | 41 | I, pu | CF card detect<br>0: Card insert<br>1: No card |
| SB1 | 32 | B | CF_IORDY/xD_D2/MS_BS/SD_D1 |
| SB2 | 33 | B | CF_RSTZ/xD_D3/MS_D1/SD_D0 |
| SB3 | 34 | B | CF_IOWZ/xD_D4/MS_D0/SD_CLK |
| SB4 | 35 | B | CF_IORZ/xD_D5/MS_D2/SD_CMD |

| | | | |
|---|---|---|---|
| SB5 | 36 | B | CF_CS1Z/xD_D6/MS_D3/SD_D3 |
| SB6 | 37 | B | CF_CS0Z/xD_D7/MS_CLK/SD_D2 |
| SB7 | 23 | B | CF_DMACK/xD_CLE/MS_D4/SD_D7 |
| SB8 | 24 | B | CF_ADR1/xD_ALE/MS_D5/SD_D6 |
| SB9 | 25 | B | CF_DMARQ/xD_D0/MS_D6/SD_D5 |
| SB10 | 26 | B | CF_ADR2/XD_D1/MS_D7/SD_D4 |
| SB11 | 27 | B | XD_WPZ/SD_WP |
| SB12 | 19 | B | CF_08/xD_RBZ |
| SB13 | 20 | B | CF_D1/xD_REZ |
| SB14 | 21 | B | CF_D0/xD_CEZ |
| SB15 | 22 | B | CF_ADR0/xD_WEZ |
| CF_D2 | 18 | B | CF Data |
| CF_D3 | 61 | B | CF Data |
| CF_D4 | 59 | B | CF Data |
| CF_D5 | 57 | B | CF Data |
| CF_D6 | 55 | B | CF Data |
| CF_D7 | 53 | B | CF Data |
| CF_D9 | 17 | B | CF Data |
| CF_D10 | 16 | B | CF Data |
| CF_D11 | 60 | B | CF Data |
| CF_D12 | 58 | B | CF Data |
| CF_D13 | 56 | B | CF Data |
| CF_D14 | 54 | B | CF Data |
| CF_D15 | 52 | B | CF Data |
| **Others** | | | |
| LED | 43 | O | Memory card access LED |
| SPI_CS | 44 | O | SPI interface: chip select |
| SPI_CK | 45 | O | SPI_CK/I2C_SCL |
| SPI_SI | 46 | O | SPI_MOSI(Connect to SPI flash data input) /I2C_SDA |
| SPI_SO | 47 | I | SPI_MISO(Connect to SPI flash data output) |
| RSTZ | 62 | I, pu | Chip reset, active low |
| TEST | 15 | | Test Pin |

**Notation:**

**Type**

| | |
|---|---|
| **O** | Output |
| **I** | Input |
| **B** | Bi-directional |
| **pu** | internal pull-up when input |
| **pd** | internal pull-down when input |
| **P** | Power / Ground |
| **A** | Analog |

**Table 3.2 – LQFN46 Pin Description**

| Pin Name | LQFN 46 Pin | Type | Description |
|---|---|---|---|
| **Power/Ground** | | | |
| AVDD12 | 3,46 | P | Analog 1.2V power source |
| AVDD33 | 9,43 | P | Analog 3.3V power source |
| DVDD12 | 21,42 | P | Digital 1.2V power source |
| DVDD33 | 31,40 | P | Digital 3.3V power source |
| V33IN | 22 | P | 3.3V to 1.2V regulator power source. Input range from 1.8V to 3.3V. |
| VUHSI | 30 | P | SD 3.0 IO PAD Power, the power source of this pin comes from the internal regulator of GL3233 and no need of external power input |
| VBUS | 38 | P | 5V Power source |
| PMOS | 39 | P | Card power 900mA |
| GND | 6 | P | Ground |
| **USB PHY Interface** | | | |
| DP | 44 | A | USB 2.0 D+ |
| DM | 45 | A | USB 2.0 D- |
| TXN | 1 | A | USB 3.0 TX- |
| TXP | 2 | A | USB 3.0 TX+ |
| RXN | 4 | A | USB 3.0 RX- |
| RXP | 5 | A | USB 3.0 RX+ |
| RTERM | 10 | A | USB reference resistor. This pin is used to control the level of USB signal. A 680ohm, 1% resistor is recommended to be populated between RTERM and GND |
| X1 | 7 | I | 25MHz XTAL input. It can be connected to external 25MHz clock input (optional) |
| X2 | 8 | B | 25MHz XTAL output (optional) |
| **Memory Card Interface** | | | |
| SD_CDZ | 20 | I, pu | SD card detect<br>0: Card insert<br>1: No card |
| MS_INS | 23 | I, pu | MS insertion detect<br>0: Card insert<br>1: No card |
| XD_CDZ | 32 | I, pu | xD card detect<br>0: Card insert<br>1: No card |
| XD_RBZ | 11 | O | xD read/busy |
| XD_REZ | 12 | O | xD read enable |
| XD_CEZ | 13 | O | xD card enable |
| XD_WEZ | 14 | O | xD write enable |

| | | | |
|---|---|---|---|
| SB1 | 24 | B | xD_D2/MS_BS/SD_D1 |
| SB2 | 25 | B | xD_D3/MS_D1/SD_D0 |
| SB3 | 26 | B | xD_D4/MS_D0/SD_CLK |
| SB4 | 27 | B | xD_D5/MS_D2/SD_CMD |
| SB5 | 28 | B | xD_D6/MS_D3/SD_D3 |
| SB6 | 29 | B | xD_D7/MS_CLK/SD_D2 |
| SB7 | 15 | B | xD_CLE/MS_D4/SD_D7 |
| SB8 | 16 | B | xD_ALE/MS_D5/SD_D6 |
| SB9 | 17 | B | xD_D0/MS_D6/SD_D5 |
| SB10 | 18 | B | xD_D1/MS_D7/SD_D4 |
| SB11 | 19 | B | SD_WP/xD_WPZ |
| **Others** | | | |
| LED | 33 | O | Memory card access LED |
| SPI_CS | 34 | O | SPI interface: chip select |
| SPI_CK | 35 | O | SPI_CK/I2C_SCL |
| SPI_SI | 36 | O | SPI_MOSI(Connect to SPI flash data input) /I2C_SDA |
| SPI_SO | 37 | I | SPI_MISO(Connect to SPI flash data output) |
| RSTZ | 41 | I, pu | Chip reset, active low |

**Notation:**

| | | |
|---|---|---|
| **Type** | **O** | Output |
| | **I** | Input |
| | **B** | Bi-directional |
| | **pu** | internal pull-up when input |
| | **pd** | internal pull-down when input |
| | **P** | Power / Ground |
| | **A** | Analog |

**Table 3.3 – LQFP48 Pin Description**

| Pin Name | LQFP 48 Pin | Type | Description |
|---|---|---|---|
| **Power/Ground** | | | |
| AVDD12 | 1,4 | P | Analog 1.2V power source |
| AVDD33 | 10,46 | P | Analog 3.3V power source |
| DVDD12 | 23,45 | P | Digital 1.2V power source |
| DVDD33 | 34,43 | P | Digital 3.3V power source |
| V33IN | 24 | P | 3.3V to 1.2V regulator power source. Input range from 1.8V to 3.3V. |
| VUHSI | 33 | P | SD 3.0 IO PAD Power, the power source of this pin comes from the internal regulator of GL3233 and no need of external power input |
| VBUS | 41 | P | 5V Power source |
| PMOS | 42 | P | Card power 900mA |
| GND | 7,22,32 | P | Ground |
| **USB PHY Interface** | | | |
| DP | 47 | A | USB 2.0 D+ |
| DM | 48 | A | USB 2.0 D- |
| TXN | 2 | A | USB 3.0 TX- |
| TXP | 3 | A | USB 3.0 TX+ |
| RXN | 5 | A | USB 3.0 RX- |
| RXP | 6 | A | USB 3.0 RX+ |
| RTERM | 11 | A | USB reference resistor. This pin is used to control the level of USB signal. A 680ohm, 1% resistor is recommended to be populated between RTERM and GND |
| X1 | 8 | I | 25MHz XTAL input. It can be connected to external 25MHz clock input (optional) |
| X2 | 9 | B | 25MHz XTAL output (optional) |
| **Memory Card Interface** | | | |
| SD_CDZ | 21 | I, pu | SD card detect<br>0: Card insert<br>1: No card |
| MS_INS | 25 | I, pu | MS insertion detect<br>0: Card insert<br>1: No card |
| XD_CDZ | 35 | I, pu | xD card detect<br>0: Card insert<br>1: No card |
| XD_RBZ | 12 | O | xD read/busy |
| XD_REZ | 13 | O | xD read enable |
| XD_CEZ | 14 | O | xD card enable |
| XD_WEZ | 15 | O | xD write enable |
| SB1 | 26 | B | XD_D2/MS_BS/SD_D1 |

| | | | |
|---|---|---|---|
| SB2 | 27 | B | XD_D3/MS_D1/SD_D0 |
| SB3 | 28 | B | XD_D4/MS_D0/SD_CLK |
| SB4 | 29 | B | XD_D5/MS_D2/SD_CMD |
| SB5 | 30 | B | XD_D6/MS_D3/SD_D3 |
| SB6 | 31 | B | XD_D7/MS_CLK/SD_D2 |
| SB7 | 16 | B | XD_CLE/MS_D4/SD_D7 |
| SB8 | 17 | B | XD_ALE/MS_D5/SD_D6 |
| SB9 | 18 | B | XD_D0/MS_D6/SD_D5 |
| SB10 | 19 | B | XD_D1/MS_D7/SD_D4 |
| SB11 | 20 | B | SD_WP/XD_WPZ |
| **Others** | | | |
| LED | 36 | O | Memory card access LED |
| SPI_CS | 37 | O | SPI interface: chip select |
| SPI_CK | 38 | O | SPI_CK/I2C_SCL |
| SPI_SI | 39 | O | SPI_MOSI(Connect to SPI flash data input) /I2C_SDA |
| SPI_SO | 40 | I | SPI_MISO(Connect to SPI flash data output) |
| RSTZ | 44 | I, pu | Chip reset, active low |

**Notation:**

**Type**

| | |
|---|---|
| **O** | Output |
| **I** | Input |
| **B** | Bi-directional |
| **pu** | internal pull-up when input |
| **pd** | internal pull-down when input |
| **P** | Power / Ground |
| **A** | Analog |

# CHAPTER 4 BLOCK DIAGRAM

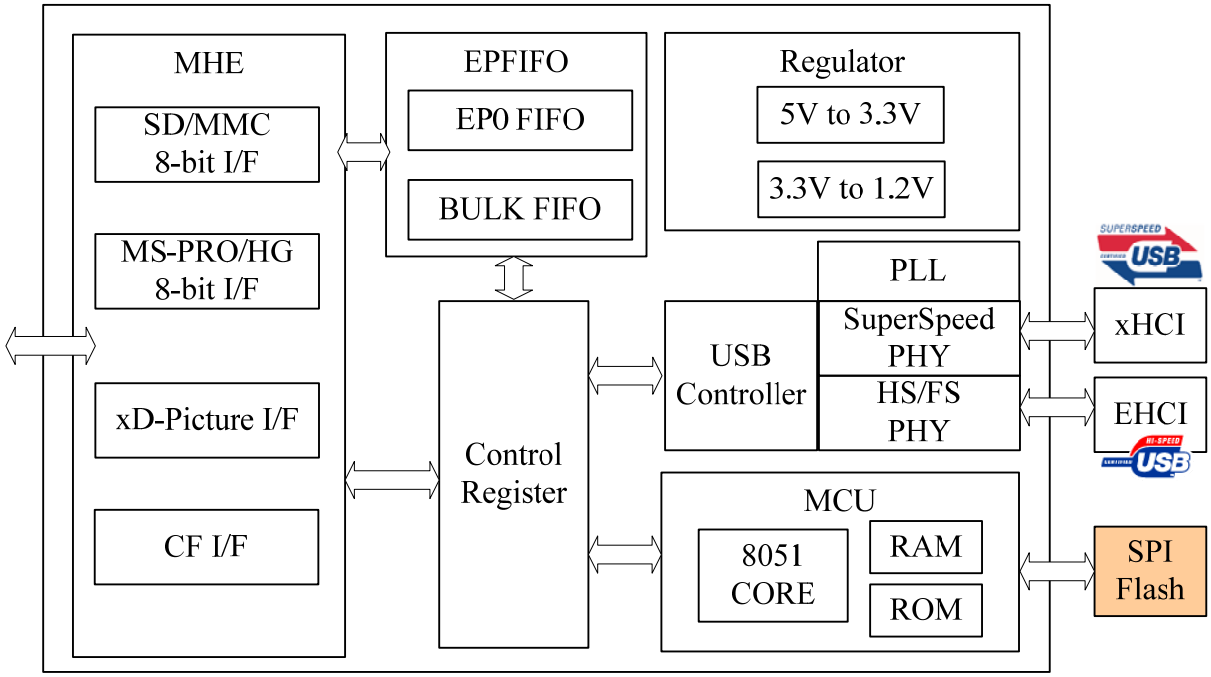


**Figure 4.1 - Functional Block Diagram**

## 4.1 Super Speed and HS/FS PHY

The transceiver macro is the analog circuitry that handles the low level USB protocol and signaling, and shifts the clock domain of the data from the USB to one that is compatible with the general logic.

## 4.2 USB Controller

The USB Controller, which contains the USB PID and address recognition logic, and other sequencing and state machine logic to handle USB packets and transactions.

## 4.3 EPFIFO

Endpoint FIFO includes Control FIFO (FIFO0) and Bulk In/Out FIFO

- **EP0 FIFO** FIFO of control endpoint 0. It is 512-byte FIFO and used for endpoint 0 data transfer.
- **Bulk In/Out FIFO** It can be in the TX mode or RX mode:
  1. It can be transmit/receive 512-byte data of USB 2.0 and 1K-byte data of USB 3.0 continuously.
  2. It can be directly accessed by micro-controller

## 4.4 MCU

8051 micro-controller inside.

- **8051 Core** Compliant with Intel 8051 high speed micro-controller
- **ROM** Firmware code on ROM
- **SRAM** Internal RAM area for MCU access

## 4.5 MHE (Media Hardware Engine)

Media Interface: CF/xD/SD/MMC/MS/MS PRO/MS PRO-HG

## 4.6 Regulator

- **5V to 3.3V 3.3V Power Source**
- **3.3V to 1.2V 1.2V Power Source**

# CHAPTER 5 ELECTRICAL CHARACTERISTICS

## 5.1 Temperature Conditions

**Table 5.1 - Temperature Conditions**

| Parameter | Value |
|---|---|
| Storage Temperature | -65°C to +150 °C |
| Operating Temperature | 0°C to +70 °C |

## 5.2 Operating Conditions

**Table 5.2 - Operating Conditions**

| Parameter | Value |
|---|---|
| Supply Voltage | +4.75V to +5.25V |
| Ground Voltage | 0V |
| $F_{OSC}$ (Oscillator or Crystal Frequency) | 25 MHz ± 0.03% |

## 5.3 DC Characteristics

**Table 5.3 - DC Characteristics**

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | | V |
| $V_{IL}$ | Input Low Voltage | | | | 0.4 | V |
| $I_I$ | Input Leakage Current | $0 < V_{IN} <$ DVDD | -10 | | 10 | μA |
| $V_{OH}$ | Output High Voltage | DVDD = 3.3V | 2.8 | | | V |
| $V_{OL}$ | Output Low Voltage | | | | 0.4 | V |
| $I_{OH}$ | Output Current High | | | 8 | | mA |
| $I_{OL}$ | Output Current Low | | | 8 | | mA |
| $C_{IN}$ | Input Pin Capacitance | | | 5 | | pF |
| $I_{NORMAL}$ | HS mode | | | 36 | | mA |
| | SS mode | U0 state | | 126 | | mA |
| | | U1 state | | 26 | | mA |
| | | U2 state | | 11 | | mA |
| $I_{ACTIVE}$ | HS mode | | | 48 | | mA |
| | SS mode | U0 state | | 138. | | mA |
| $I_{RESET}$ | | | | 32 | | mA |
| $I_{SUS}$ | HS suspend current | 1.5K pull-up included | | 0.82 | | mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| | SS suspend current | U3 state | | 0.7 | | mA |
| $R_{pu}$ | Reset Pad pull-up | | | 46 | | KΩ |
| | SD_CDZ, SD_WP, MS_INS, GPIO Pad pull-up | | | 46 | | KΩ |
| | SD_CMD pull-up | | | 15 | | KΩ |
| | SD_CLK, D[3:0] Pad pull-up | | | 15 | | KΩ |
| $R_{IMP}$ | SD_CMD, SD_CLK, D[3:0] impedances | | | 50 | | Ω |

## 5.4 AC Characteristics of Reset Timing

### 5.4.1 Reset Timing

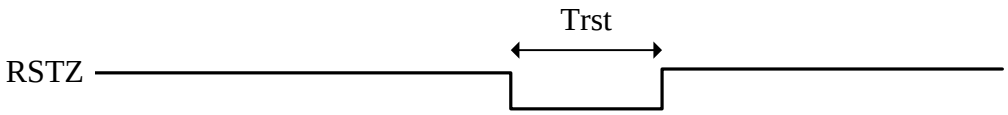


**Figure 5.1 - Timing Diagram of Reset Width**

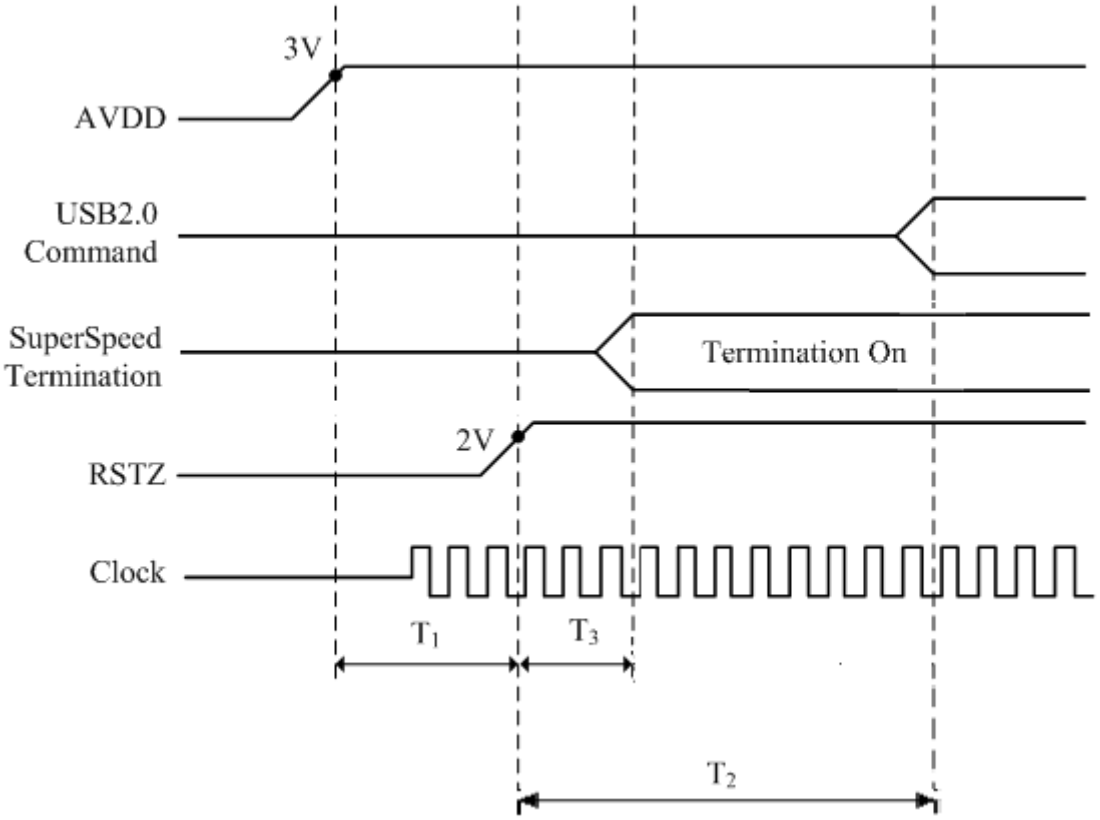


**Figure 5.2 - Timing Diagram of Power Good to USB Command Receive Ready**

**Table 5.4 - Reset Timing**

| Parameter | Description | Min. | Unit |
|---|---|---|---|
| Trst | Chip reset sense timing width | 2 | us |
| T1 | AVDD power up to reset de-assert | 500 | us |
| T2 | Reset de-assert to respond USB2.0 command ready | 95 | ms |
| T3 | Reset de-assert to SuperSpeed termination on | 12 | ms |

### 5.4.2 SD/MMC Card Clock Frequency

**Table 5.5 - SD/MMC Card Clock Frequency**

| Parameter | Description | Max. | Unit |
|---|---|---|---|
| $F_{ID}$ | Clock frequency Identification Mode | 187 | KHz |
| $F_{DS}$ | Clock frequency Default Speed Mode | 25 | MHz |
| $F_{HS}$ | SD Clock frequency High Speed Mode | 50 | MHz |
| $F_{HS}$ | MMC Clock frequency High Speed Mode | 52 | MHz |
| $F_{SDR25}$ | Clock frequency Ultra High Speed Mode: SDR25 | 50 | MHz |
| $F_{DDR50}$ | Clock frequency Ultra High Speed Mode: DDR50 | 50 | MHz |
| $F_{SDR50}$ | Clock frequency Ultra High Speed Mode: SDR50 | 100 | MHz |
| $F_{SDR104}$ | Clock frequency Ultra High Speed Mode: SDR104 | 208 | MHz |

### 5.4.3 MS Card Clock Frequency

**Table 5.6 - MS Card Clock Frequency**

| Parameter | Description | Max. | Unit |
|---|---|---|---|
| $F_{DS}$ | Clock frequency Default Speed Mode | 20 | MHz |
| $F_{MSP}$ | Clock frequency MS PRO 4bit Mode | 40 | MHz |
| $F_{MSPHG}$ | Clock frequency MS PRO HG 8bit Mode | 60 | MHz |

# CHAPTER 6 SPI NOR FLASH SUPPORT LIST

**Table 6.1 - SPI NOR Flash Support List**

| Vendor | Model |
|---|---|
| GigaDevice | GD25Q512 |
| | GD25Q010 |
| PMC | PM25LD512C |
| | PM25LD010 |
| | PM25LD010C |
| | PM25LD020 |
| | PM25LD020C |
| | PM25LV010(*) |
| WINBON | W25X05CL |
| | W25X10CL |
| | W25X10BV |
| | W25X20CL |
| | W25X20BV |
| EON | EN25F10(*) |
| | EN25LF10(*) |
| | EN25Q40 |
| MXIC | MX25L1006E |
| | MX25L5121E(*) |
| | MX25L512C(*) |
| ATMEL | AT25F512B(*) |

**Note** :

- GL3233 support Page-Porgram SPI Flash only, not for Byte-program SPI Flash
- (*) are listed as standard SPI Flash model, others are listed as dual SPI Flash model, Genesys Logic recommand adopting dual SPI Flash for better Read Write performance
- Firmware file (xxxx.bin) which Genesys Logic provided is only used for Genesys Logic's Multi-Tool and MP Tool ISP (In System Programming via USB interface) purpose. If you would like to provide FW for SPI Flash vendor mass production or Flash ROM writer, please contact with GL technical support team.

# CHAPTER 7 PACKAGE DIMENSION

| SYMBOL | DIMENSION MM (MIL) | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.60 (63.0) |
| A1 | 0.05 (2.0) | --- | 0.15 (5.9) |
| A2 | 1.35 (53.1) | 1.40 (55.1) | 1.45 (57.1) |
| b | 0.13 (5.1) | 0.18 (7.1) | 0.23 (9.1) |
| b1 | 0.13 (5.1) | 0.16 (6.3) | 0.19 (7.5) |
| c | 0.09 (3.5) | --- | 0.20 (7.9) |
| c1 | 0.09 (3.5) | --- | 0.16 (6.3) |
| D | 9.00 (354.3) BSC | | |
| D1 | 7.00 (275.6) BSC | | |
| e | 0.40 (15.7) BSC | | |
| E | 9.00 (354.3) BSC | | |
| E1 | 7.00 (275.6) BSC | | |
| L | 0.45 (17.7) | 0.60 (23.6) | 0.75 (29.5) |
| L1 | 1.00 (39.4) REF | | |
| R1 | 0.08 (3.1) | --- | --- |
| R2 | 0.08 (3.1) | --- | 0.20 (7.9) |
| S | 0.20 (7.9) | --- | --- |
| aaa | 0.20 (7.9) | | |
| bbb | 0.20 (7.9) | | |
| ccc | 0.08 (3.1) | | |
| ddd | 0.07 (2.8) | | |
| θ | 0° | 3.5° | 7° |
| θ1 | 0° | --- | --- |
| θ2 | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° |

NOTE: 1. REFER TO JEDEC MS-026/BBD
2. ALL DIMENSIONS IN MILLIMETERS.

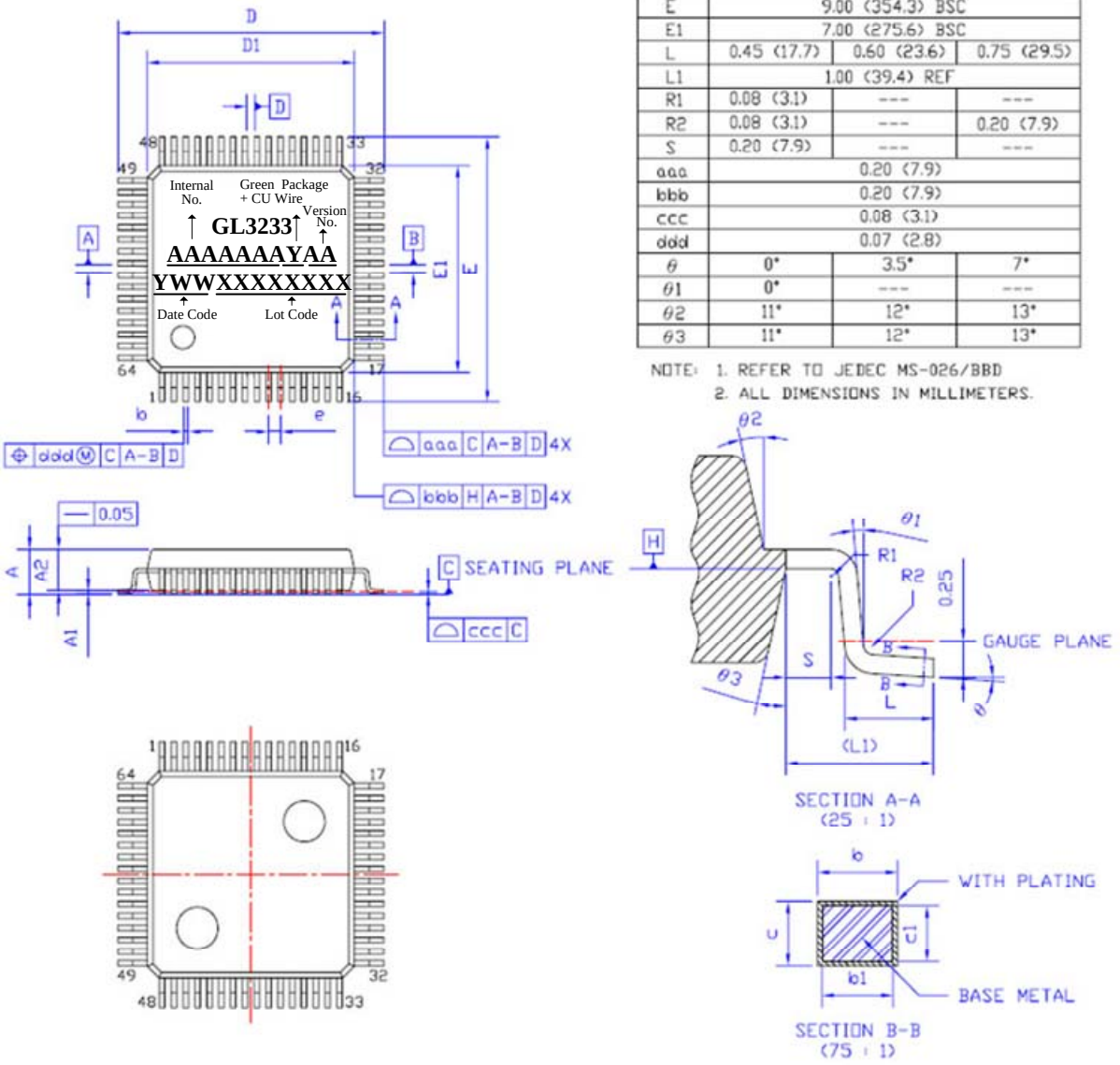


**Figure 7.1 - LQFP 64 Pin Package**

| SYMBOL | DIMENSION MM (MIL) | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.60 (23.6) | 0.66 (26.0) | 0.80 (31.5) |
| A1 | --- | 0.02 (0.8) | 0.05 (2.0) |
| A3 | 0.11 (4.3) | 0.20 (7.9) | 0.26 (10.2) |
| b | 0.13 (5.1) | 0.20 (7.9) | 0.25 (9.8) |
| D | 6.50 (255.9) BSC | | |
| D2 | 4.95 (194.9) | 5.10 (200.8) | 5.25 (206.7) |
| E | 4.50 (177.2) BSC | | |
| E2 | 2.95 (116.1) | 3.10 (122.0) | 3.25 (128.0) |
| e | 0.40 (15.7) BSC | | |
| L | 0.30 (11.8) | 0.40 (15.7) | 0.50 (19.7) |

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

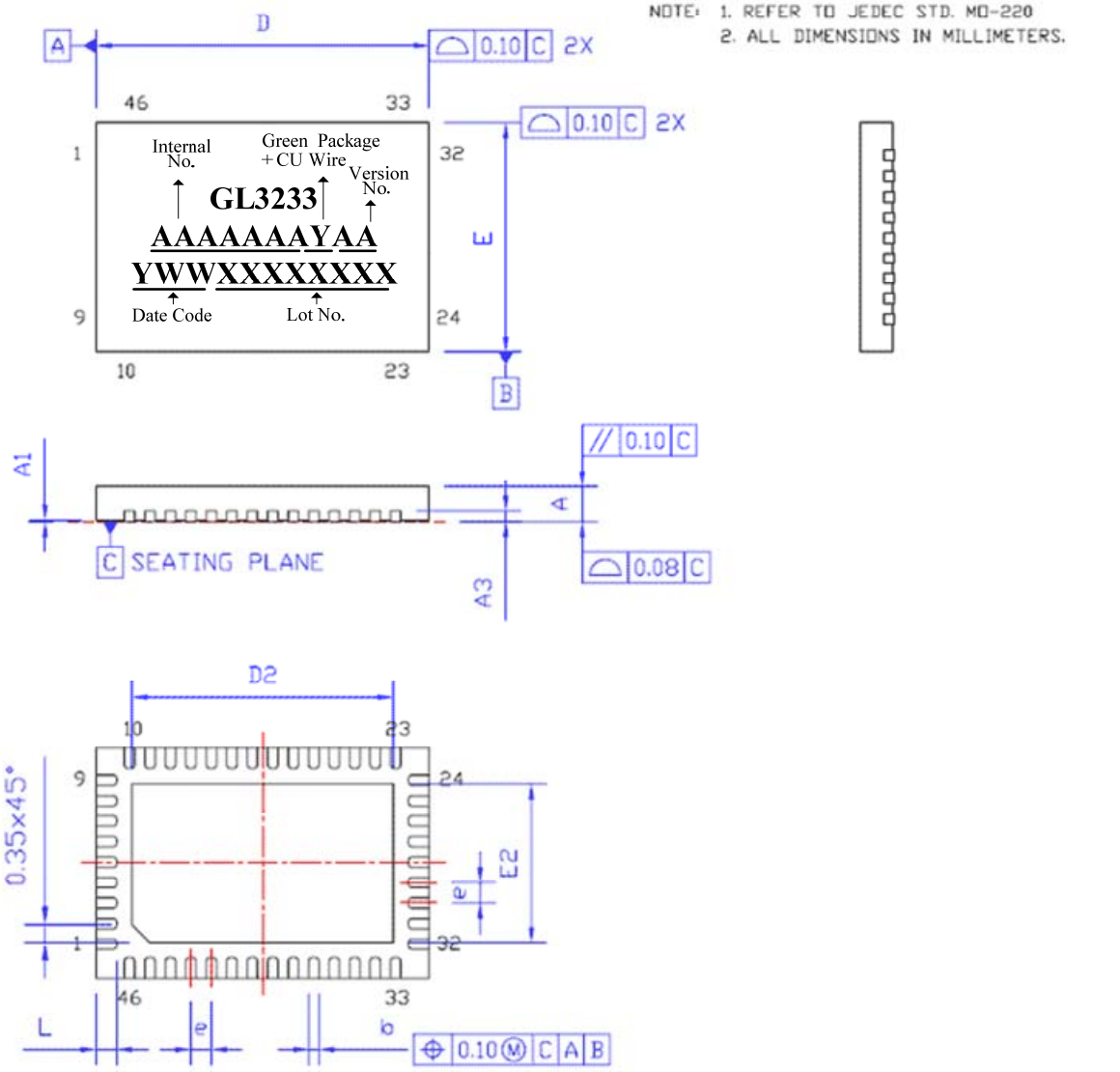


**Figure 7.2 - LQFN 46 Pin Package**

| SYMBOL | DIMENSION MM (MIL) | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.60 (63.0) |
| A1 | 0.05 (2.0) | --- | 0.15 (5.9) |
| A2 | 1.35 (53.1) | 1.40 (55.1) | 1.45 (57.1) |
| b | 0.17 (6.7) | 0.22 (8.7) | 0.27 (10.6) |
| b1 | 0.17 (6.7) | 0.20 (7.9) | 0.23 (9.1) |
| c | 0.09 (3.5) | --- | 0.20 (7.9) |
| c1 | 0.09 (3.5) | --- | 0.16 (6.3) |
| D | 9.00 (354.3) BSC | | |
| D1 | 7.00 (275.6) BSC | | |
| e | 0.50 (19.7) BSC | | |
| E | 9.00 (354.3) BSC | | |
| E1 | 7.00 (275.6) BSC | | |
| L | 0.45 (17.7) | 0.60 (23.6) | 0.75 (29.5) |
| L1 | 1.00 (39.4) REF | | |
| R1 | 0.08 (3.1) | --- | --- |
| R2 | 0.08 (3.1) | --- | 0.20 (7.9) |
| S | 0.20 (7.9) | --- | --- |
| aaa | 0.20 (7.9) | | |
| bbb | 0.20 (7.9) | | |
| ccc | 0.08 (3.1) | | |
| ddd | 0.08 (3.1) | | |
| θ | 0° | 3.5° | 7° |
| θ1 | 0° | --- | --- |
| θ2 | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° |

NOTE: 1. REFER TO JEDEC MS-026/BBC
2. ALL DIMENSIONS IN MILLIMETERS.

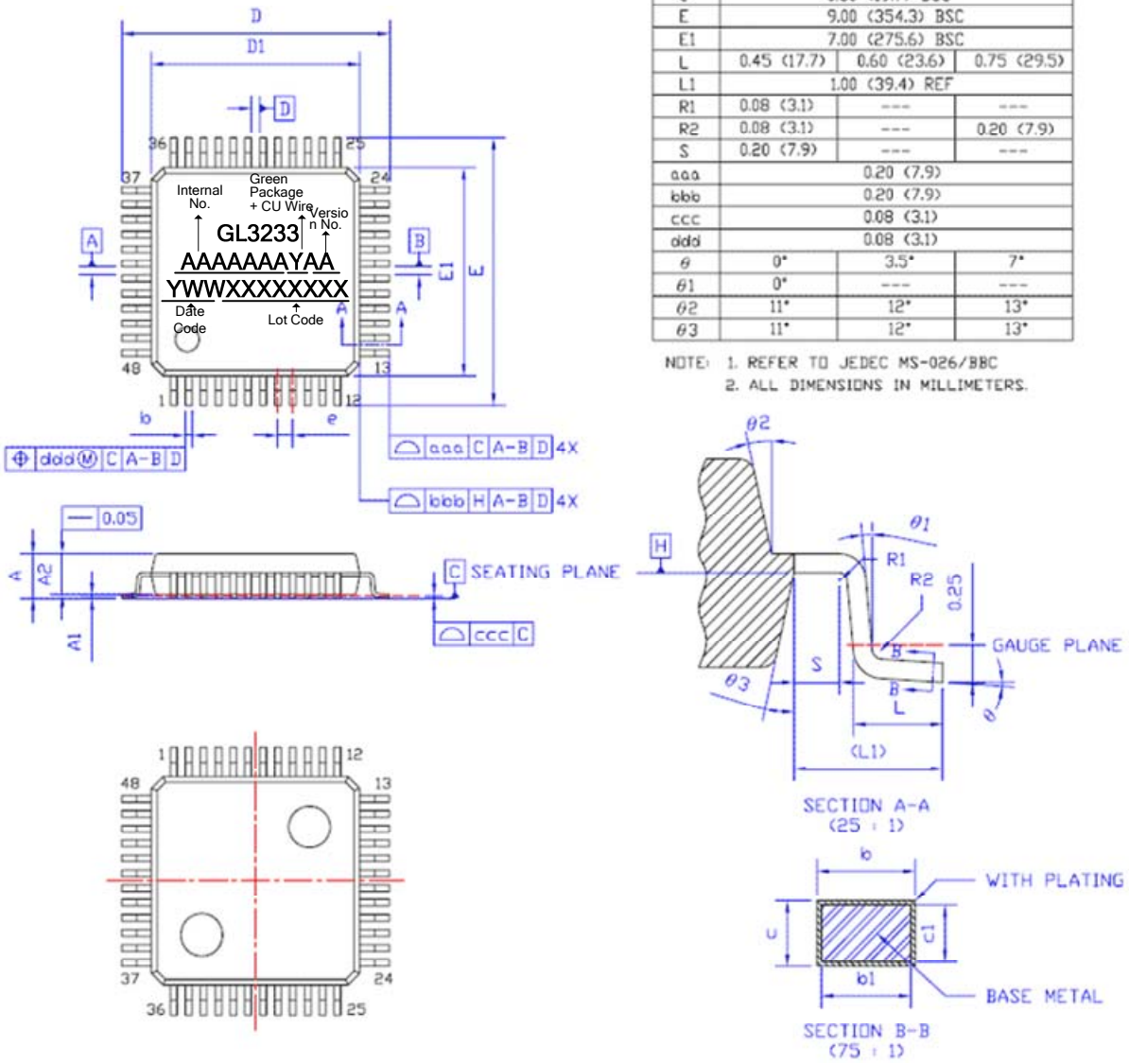


**Figure 7.3 - LQFP 48 Pin Package**

# CHAPTER 8 ORDERING INFORMATION

**Table 8.1 - Ordering Information**

| Part Number | Package | Green/Wire Material | Version | Status |
|---|---|---|---|---|
| GL3233-MSYXX | LQFP 64 | Green Package + CU Wire | XX | Available |
| GL3233-PMYXX | LQFN 46 | Green Package + CU Wire | XX | Available |
| GL3233-MNYXX | LQFP 48 | Green Package + CU Wire | XX | Available |